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L1 and ((increas$3 or decreas$3) same (process$3 adj1 activity))	12

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L1	monitor$3 near10 (process$3 adj1 activity)	142	L1

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L3	L2	0	L3
DB=USPT; PLUR=YES; OP=OR			
L2	L1 and ((increas$3 or decreas$3) same (process$3 adj1 activity))	12	L2
L1	monitor$3 near10 (process$3 adj1 activity)	142	L1

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Search Results -

Terms	Documents
(361/323 |361/683 |307/60 |340/636 |713/320 |713/321 |713/322 |713/323 |713/501 |713/600 |713/300).ccls.	5206

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DATE: Monday, May 17, 2004 Printable Copy Create Case

Set Name side by side	Query	Hit Count	Set Name result set
	DB=USPT,USOC; PLUR=YES; OP=OR		
L1	713/320-323,501,600,300;361/323,683;340/636;307/60.ccls.	5206	L1

END OF SEARCH HISTORY

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Search Results -

Terms	Documents
L1 and L2	13

Database:
US Pre-Grant Publication Full-Text Database
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Derwent World Patents Index
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Search: L4

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DB=USPT,USOC; PLUR=YES; OP=OR			
L4	l1 and l2	13	L4
L3	L2 and ((increas$3 or decreas$3) same (process$3 adj1 activity))	12	L3
L2	monitor$3 near10 (process$3 adj1 activity)	143	L2
L1	713/320-323,501,600,300;361/323,683;340/636;307/60.ccls.	5206	L1

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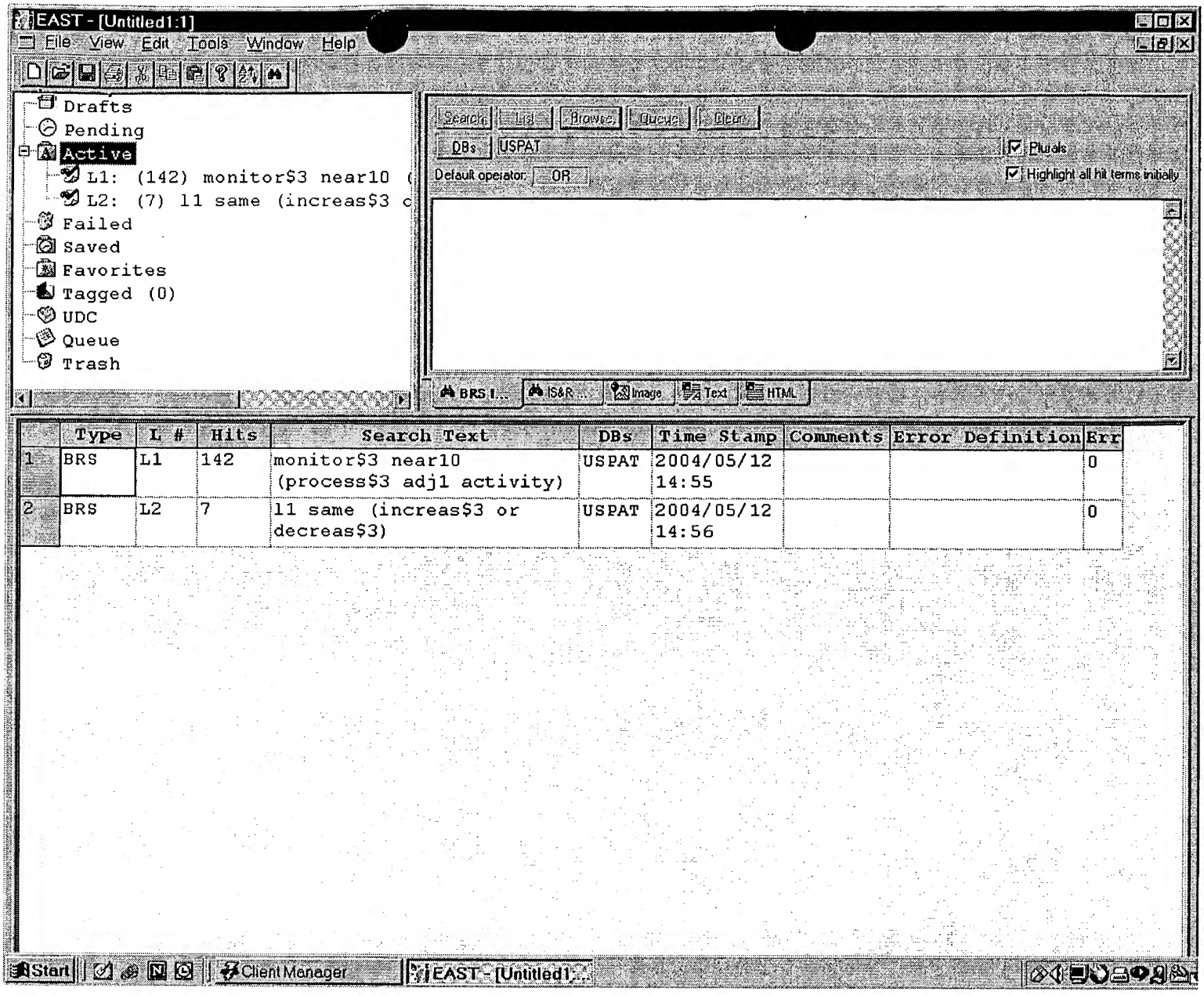

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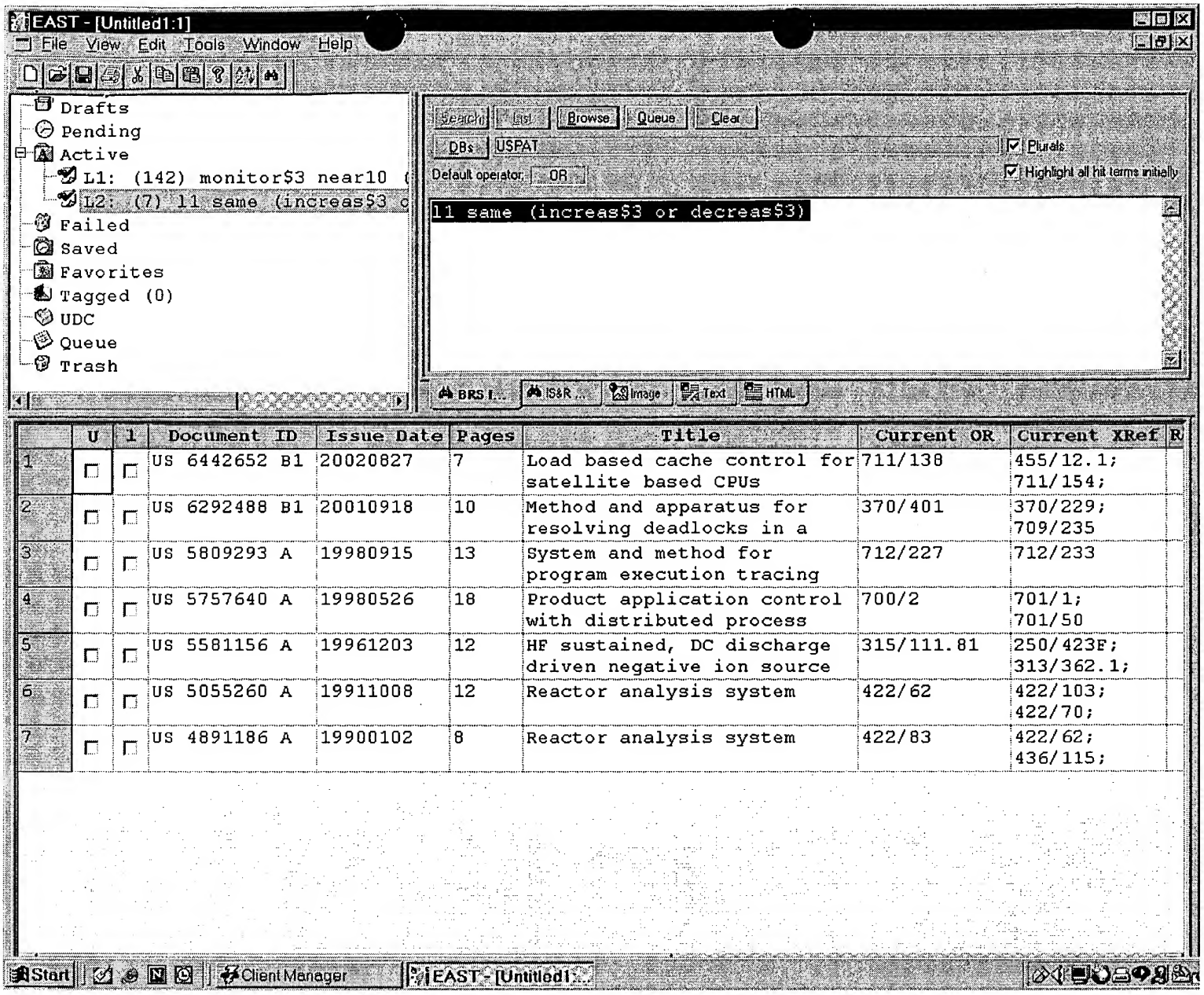

	U	1	Document ID	Issue Date	Pages	Title	Current OR	Current XRef	R
1	☐	☐	US 6442652 B1	20020827	7	Load based cache control for satellite based CPUs	711/138	455/12.1; 711/154;	
2	☐	☐	US 6292488 B1	20010918	10	Method and apparatus for resolving deadlocks in a	370/401	370/229; 709/235	
3	☐	☐	US 5809293 A	19980915	13	System and method for program execution tracing	712/227	712/233	
4	☐	☐	US 5757640 A	19980526	18	Product application control with distributed process	700/2	701/1; 701/50	
5	☐	☐	US 5581156 A	19961203	12	HF sustained, DC discharge driven negative ion source	315/111.81	250/423F; 313/362.1;	
6	☐	☐	US 5055260 A	19911008	12	Reactor analysis system	422/62	422/103; 422/70;	
7	☐	☐	US 4891186 A	19900102	8	Reactor analysis system	422/83	422/62; 436/115;	

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1 **Improving the data cache performance of multiprocessor operating systems**
Chun Xia; Torrellas, J.;
High-Performance Computer Architecture, 1996. Proceedings. Second Interna Symposium on , 3-7 Feb. 1996
Pages:85 - 94

[Abstract] [PDF Full-Text (1084 KB)] **IEEE CNF**

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2 **Interfield Hybrid Coding of Component Color Television Signals**
Kamangar, F.; Rao, K.;
Communications, IEEE Transactions on [legacy, pre - 1988] , Volume: 29 , Is 12 , Dec 1981
Pages:1740 - 1753

[Abstract] [PDF Full-Text (1576 KB)] **IEEE JNL**

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3 **Hardware evaluation of low power communication mechanisms for transport-triggered architectures**
Pionteck, T.; Garcia, A.; Kabulepa, L.D.; Glesner, M.;
Rapid Systems Prototyping, 2003. Proceedings. 14th IEEE International Work on , 9-11 June 2003
Pages:141 - 147

[Abstract] [PDF Full-Text (303 KB)] **IEEE CNF**

---

4 **A multifrequency laboratory investigation of attenuation and scatte from volcanic ash clouds**
Bredow, J.W.; Porco, R.; Dawson, M.S.; Betty, C.L.; Self, S.; Thordarson, T.;
Geoscience and Remote Sensing, IEEE Transactions on , Volume: 33 , Issue:

4 , July 1995
Pages:1071 - 1082

[Abstract] [PDF Full-Text (896 KB)] **IEEE JNL**

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5 **Satellite-based data telemetry and geolocation Argos enhancement the coastal ocean**
Wingenroth, J.;
OCEANS '96. MTS/IEEE. 'Prospects for the 21st Century'. Conference Proceedings , Volume: 1 , 23-26 Sept. 1996
Pages:272 - 276 vol.1

[Abstract] [PDF Full-Text (460 KB)] **IEEE CNF**

---

6 **Data acquisition device with packet based communication protocol engine monitoring**
Alonso, R.E.; Leffew, J.; Shreinivasan, S.; Moreno, W.;
Devices, Circuits and Systems, 2002. Proceedings of the Fourth IEEE Internat Caracas Conference on , 17-19 April 2002
Pages:I029 - I1-5

[Abstract] [PDF Full-Text (459 KB)] **IEEE CNF**

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7 **Finding good peers in peer-to-peer networks**
Krishna Ramanathan, M.; Kalogeraki, V.; Pruyne, J.;
Parallel and Distributed Processing Symposium., Proceedings International, IF 2002, Abstracts and CD-ROM , 15-19 April 2002
Pages:24 - 31

[Abstract] [PDF Full-Text (314 KB)] **IEEE CNF**

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8 **Everyday monitoring of the operators' psychophysiological safety**
Sikorsky, E.A.; Burov, A.Yu.;
Digital Avionics Systems Conference, 1999. Proceedings. 18th , Volume: 2 , 2 Oct. 1999
Pages:6.D.5-1 - 6.D.5-4 vol.2

[Abstract] [PDF Full-Text (236 KB)] **IEEE CNF**

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Improving the data cache performance of multiprocessor operating systems

Chun Xia Torrellas, J.
Center for Supercomput. Res. & Dev., Illinois Univ., Urbana, IL, USA;

This paper appears in: **High-Performance Computer Architecture, 1996. Proceedings. Second International Symposium on**

Meeting Date: 02/03/1996 - 02/07/1996
Publication Date: 3-7 Feb. 1996
Location: San Jose, CA USA
On page(s): 85 - 94
Reference Cited: 20
Inspec Accession Number: 5257142

Abstract:
Bus-based shared-memory multiprocessors with coherent caches have recently become very popular. To achieve high **performance**, these systems rely on **increasingly** sophisticated cache hierarchies. However, while these machines often run loads with substantial operating system **activity**, **performance** measurements have consistently indicated that the operating system uses the data cache hierarchy poorly. In this paper, we address the issue of how to eliminate most of the data cache misses in a multiprocessor operating system while still using off-the-shelf **processors**. We use a

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performance monitor to examine traces of a 4-**processor** machine running four system-intensive loads under UNIX. Based on our observations, we propose hardware and software support that targets block operations, coherence **activity**, and cache conflicts. For block operations, simple cache bypassing or prefetching schemes are undesirable. Instead, it is best to use a DMA-like scheme that pipelines the data transfer in the bus without involving the **processor**. Coherence misses are handled with data, privatization and relocation, and the use of updates for a small core of shared variables. Finally, the remaining miss hot spots are handled with data prefetching. Overall, our simulations show that all these optimizations combined eliminate or hide 75% of the operating system data misses in 32-Kbyte primary caches. Furthermore, they speed up the operating system by 19%

Index Terms:

cache storage **performance** evaluation shared memory systems 4-**processor** machine DMA-like scheme coherence **activity** coherent caches data cache **performance** data transfer multiprocessor operating systems **performance** measurements **performance monitor** shared-memory multiprocessors

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Finding good peers in peer-to-peer networks

Krishna Ramanathan, M. Kalogeraki, V. Pruyne, J.
Dept. of Comput. Sci., Purdue Univ., West Lafayette, IN, USA;

This paper appears in: **Parallel and Distributed Processing Symposium., Proceedings International, IPDPS 2002, Abstracts and CD-ROM**

Meeting Date: 04/15/2002 - 04/19/2002
Publication Date: 15-19 April 2002
Location: Ft. Lauderdale, FL USA
On page(s): 24 - 31
Reference Cited: 15
Number of Pages: CD-ROM
Inspec Accession Number: 7342315

Abstract:
As computing and communication capabilities have continued to **increase**, more and more **activity** is taking place at the edges of the network, typically in homes or on workers desktops. This trend has been demonstrated by the **increasing** popularity and usability of "peer-to-peer" systems, such as Napster and Gnutella. Unfortunately, this popularity has quickly shown the limitations of these systems, particularly in terms of scale. Because the networks form in an ad-hoc manner, they typically make inefficient use of resources. We propose a mechanism, using only local knowledge, to improve the

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overall **performance** of peer-to-peer networks based on interests. Peers **monitor** which other peers frequently respond successfully to their requests for information. When a peer is discovered to frequently provide good results, the peer attempts to move closer to it in the network by creating a new connection with that peer. This leads to clusters of peers with similar interests, and in turn allows us to limit the depth of searches required to find good results. We have implemented our algorithm in the context of a distributed encyclopedia-style information-sharing application which is built on top of the Gnutella network. In our testing environment, we have shown the ability to greatly reduce the amount of communication resources required to find the desired articles in the encyclopedia

Index Terms:

distributed algorithms electronic data interchange encyclopaedias information networks user modelling Gnutella Napster ad-hoc networks communication resources distributed encyclopedia-style information-sharing application inefficient resource use information requests local knowledge network **performance** peer clusters peer finding peer interests peer **monitoring** peer-to-peer connections peer-to-peer networks search depth testing environment

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☐ 1. Document ID: US 6691237 B1

Using default format because multiple data bases are involved.

L4: Entry 1 of 13 File: USPT Feb 10, 2004

US-PAT-NO: 6691237
DOCUMENT-IDENTIFIER: US 6691237 B1

TITLE: Active memory pool management policies

DATE-ISSUED: February 10, 2004

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Verdun; Gary J.	Belton	TX		
Roesle; Chad P.	Austin	TX		

US-CL-CURRENT: 713/320; 711/170

Full | Title | Citation | Front | Review | Classification | Date | Reference | Claims | KWIC | Draw De

☐ 2. Document ID: US 6564328 B1

L4: Entry 2 of 13 File: USPT May 13, 2003

US-PAT-NO: 6564328
DOCUMENT-IDENTIFIER: US 6564328 B1
** See image for Certificate of Correction **

TITLE: Microprocessor with digital power throttle

Full | Title | Citation | Front | Review | Classification | Date | Reference | Claims | KWIC | Draw De

☐ 3. Document ID: US 6487668 B2

L4: Entry 3 of 13 File: USPT Nov 26, 2002

US-PAT-NO: 6487668
DOCUMENT-IDENTIFIER: US 6487668 B2
** See image for Certificate of Correction **

h e b b g e e e f e g ef b e

TITLE: Thermal and power management to computer systems

Full | Title | Citation | Front | Review | Classification | Date | Reference | Claims | KWMC | Draw De

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☐ 4. Document ID: US 6397343 B1

L4: Entry 4 of 13 File: USPT May 28, 2002

US-PAT-NO: 6397343
DOCUMENT-IDENTIFIER: US 6397343 B1
** See image for Certificate of Correction **

TITLE: Method and system for dynamic clock frequency adjustment for a graphics subsystem in a computer

Full | Title | Citation | Front | Review | Classification | Date | Reference | Claims | KWMC | Draw De

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☐ 5. Document ID: US 6216235 B1

L4: Entry 5 of 13 File: USPT Apr 10, 2001

US-PAT-NO: 6216235
DOCUMENT-IDENTIFIER: US 6216235 B1

TITLE: Thermal and power management for computer systems

Full | Title | Citation | Front | Review | Classification | Date | Reference | Claims | KWMC | Draw De

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☐ 6. Document ID: US 5974557 A

L4: Entry 6 of 13 File: USPT Oct 26, 1999

US-PAT-NO: 5974557
DOCUMENT-IDENTIFIER: US 5974557 A

TITLE: Method and system for performing thermal and power management for a computer

Full | Title | Citation | Front | Review | Classification | Date | Reference | Claims | KWMC | Draw De

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☐ 7. Document ID: US 5931950 A

L4: Entry 7 of 13 File: USPT Aug 3, 1999

US-PAT-NO: 5931950
DOCUMENT-IDENTIFIER: US 5931950 A

TITLE: Wake-up-on-ring power conservation for host signal processing communication system

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Full | Title | Citation | Front | Review | Classification | Date | Reference | Claims | KWIC | Draw De

☐ 8. Document ID: US 5913067 A

L4: Entry 8 of 13 File: USPT Jun 15, 1999

US-PAT-NO: 5913067
DOCUMENT-IDENTIFIER: US 5913067 A
** See image for Certificate of Correction **

TITLE: Apparatus for adaptive power management of a computer system

Full | Title | Citation | Front | Review | Classification | Date | Reference | Claims | KWIC | Draw De

☐ 9. Document ID: US 5784598 A

L4: Entry 9 of 13 File: USPT Jul 21, 1998

US-PAT-NO: 5784598
DOCUMENT-IDENTIFIER: US 5784598 A
** See image for Certificate of Correction **

TITLE: Method and apparatus for changing processor clock rate

Full | Title | Citation | Front | Review | Classification | Date | Reference | Claims | KWIC | Draw De

☐ 10. Document ID: US 5758175 A

L4: Entry 10 of 13 File: USPT May 26, 1998

US-PAT-NO: 5758175
DOCUMENT-IDENTIFIER: US 5758175 A

TITLE: Multi-mode power switching for computer systems

Full | Title | Citation | Front | Review | Classification | Date | Reference | Claims | KWIC | Draw De

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Terms	Documents
L1 and L2	13

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L1: Entry 1 of 1 File: USPT Jun 2, 1987

DOCUMENT-IDENTIFIER: US 4670837 A

** See image for Certificate of Correction **

TITLE: Electrical system having variable-frequency clock

Detailed Description Text (9):

It is to be understood that the above-described embodiment is merely illustrative of the principles of the present invention and that other embodiments may be devised by those skilled in the art without departing from the spirit and scope of the invention. For example, the LC oscillator implementation of digital VCO 102 may be replaced by a switched RC oscillator where resistors of differing resistance are switched in and out of the circuit to vary the frequency in response to the digital words received by the D/A converter. Rather than computing the frequency based on the processing backlog, the activity on data bus 104 and address bus 105 could be monitored and then used as a basis for determining the required frequency. Instead of using a continuously variable-frequency clock, selections can be made from a small number of discrete frequencies. For example, in a battery-powered personal computer with an operating system which includes a sleep state, the microprocessor CPU could be operated at a low frequency sufficient to keep any dynamic logic refreshed, e.g., 500 kilohertz, when the operating system is in the sleep state, and the frequency could then be increased to a nominal operating frequency, e.g., 10 megahertz, when wakeup occurs. In some applications, the desired clock frequency could be determined based on historical activity records rather than in real time. For example, the operating frequency of the distributed microprocessors used for control in a telephone switching system could be adjusted based on calling patterns observed during different times of the day or during different days of the week as a way of reducing the energy requirements of the system. It is to be recognized that any of a number of microprocessor families can be advantageously used in such systems. One specific example is the Motorola 68000 microprocessor and its associated devices. Furthermore, the invention is applicable to clocked, electrical systems other than microprocessor-based systems where power consumption is a function of clock frequency as, for example, in gate arrays.

First Hit Fwd Refs

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L5: Entry 1 of 1 File: USPT Jun 8, 1993

DOCUMENT-IDENTIFIER: US 5218704 A

**** See image for Certificate of Correction ****

TITLE: Real-time power conservation for portable computers

Brief Summary Text (7):

However, the software developed was desiged to run on desk top personal computers, with all the features of desk top computers, without regard to battery-powered portable computers that only had limited amounts of power available for short periods of time. No special considerations were made by the software, operating system (MS-DOS), Basic Input/Output System (BIOS), or the third party application software to conserve power usage for these portable computers.

Detailed Description Text (40):

Looking now at FIG. 4, which depicts a schematic of an actual sleep hardware implementation for a system such as the Intel 80386 (CPU cannot have its clock stopped). Address enable bus 600 and address bus 610 provide CPU input to demultiplexer 620. The output of demultiplexer 620 is sent along SLEEPCS- and provided as input to OR gates 630,640. The other inputs to OR gates 630,640 are the I/O write control line and the I/O read control line, respectively. The outputs of these gates, in addition to NOR gate 650, are applied to D flip flop 660 to decode the port. "INTR" is the interrupt input from the I/O port (peripherals) into NOR gate 650, which causes the logic hardware to switch back to the high speed clock. The output of flip flop 660 is then fed, along with the output from OR gate 630, to tristate buffer 670 to enable it to read back what is on the port. All of the above-identified hardware is used by the read/write I/O port (peripherals) to select the power saving "Sleep" operation. The output "SLOW-" is equivalent to "SLEEP" in FIG. 2, and is inputted to flip flop 680, discussed later.

CLAIMS:

5. The method for real-time power conservation of claim 1, wherein said step (a) of determining whether a central processing unit (CPU) in a computer is available for power conservation, further comprises the steps of:

checking to see if said CPU has received a request;

if said CPU has received a request, determining whether said request is a critical input/output;

preventing said CPU from entering said power conservation mode if said request is a critical input/output;

if said request is not a critical input/output, determining whether there are any interrupts available to wake said CPU before said CPU enters said power conservation mode;

preventing said CPU from entering said power conservation mode;

determining whether said request is from an input/output having a delay intil the I/O device become ready; and

prevent said CPU from entering said power conservation mode if said request is not from an input/output having a delay.

12. The apparatus for power conservation of claim 9, wherein said CPU activity detector further comprises:

a detector for detecting a first rate of critical input/output interrupts and a second rate of critical input/output interrupts received by said CPU;

a comparator for comparing said detected first rate with said detected second rate and determining whether said detected rate has increased;

an indicator for indicating a current CPU activity level based on a determination received from said comparator; and

a designator for receiving said indicated current CPU activity level and communicating said indicated current CPU activity level to said CPU sleep manager.

L2: Entry 1 of 12 File: USPT Nov 26, 2002

DOCUMENT-IDENTIFIER: US 6487668 B2
**** See image for Certificate of Correction ****
TITLE: Thermal and power management to computer systems

Brief Summary Text (20):
The invention may be implemented as an apparatus or a method. According to one embodiment, the invention monitors a processor's activity and its temperature. When there is no activity for the processor, a slowed clock frequency is used, thereby saving power and lowering the thermal heat produced by the processor. On the other hand, when there is activity for the processor, a fast clock frequency is used. However, when prolonged activity (i.e., sustained fast clock frequency) causes the processor's temperature to become dangerously high for proper operation, the clock frequency is reduced so as to maintain processing speed at a reduced speed while preventing overheating.

Detailed Description Text (3):
The invention monitors a processor's activity and its temperature. When there is no activity for the processor, a slow clock frequency is used, thereby saving power and lowering the thermal heat produced by the processor. On the other hand, when there is activity for the processor, a fast clock frequency is used. However, when prolonged activity (i.e., sustained fast clock frequency) causes the processor's temperature to become dangerously high for proper operation, the clock frequency is reduced so as to maintain processing speed at a reduced speed while preventing overheating.

Detailed Description Text (26):
Prior embodiments operate to decrease the clock frequency of the clock signals supplied to a microprocessor to prevent overheating and to conserve energy. FIG. 10 is a block diagram of a seventh embodiment of the invention. This embodiment operates to provide a burst processing mode for use under certain conditions. During certain types of processing activity, a clock control unit 20 causes an overdrive clock to be supplied to a microprocessor 2. Because the overdrive clock is used only in short bursts, the frequency of the overdrive clock can and preferably exceeds the frequency which sustained processing would permit without rapidly overheating.

CLAIMS:

6. A computer, comprising: a processor, said processor processes instructions in accordance with a clock signal; an activity detector operatively connected to said processor, said activity detector monitors activity of said processor, said activity detector determines whether said processor is in normal power mode or a reduced power mode; a fan; and a fan controller, said fan controller controls the speed of said fan in accordance with the activity of said processor such that the speed of said fan is less utilized when said processor is in the reduced power mode than when said processor is in the normal power mode.

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L2: Entry 1 of 12 File: USPT Nov 26, 2002

US-PAT-NO: 6487668
DOCUMENT-IDENTIFIER: US 6487668 B2
** See image for Certificate of Correction **

TITLE: Thermal and power management to computer systems

DATE-ISSUED: November 26, 2002

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Thomas; C. Douglass	Campbell	CA	95008	
Thomas; Alan E.	Ocean City	NJ	08226	

APPL-NO: 09/ 782680 [PALM]
DATE FILED: February 12, 2001

PARENT-CASE:
CROSS REFERENCE TO RELATED APPLICATIONS This application is a continuation application of prior U.S. Application No. 09/351,051 filed on Jul. 10, 1999, now U.S. Pat. No. 6,216,235, which is a continuation application of U.S. application No. 08/914,299 filed on Aug. 18, 1997, now U.S. Pat. No. 5,974,557, which is a continuation application of U.S. application No.08/262,754 filed Jun. 20, 1994, now U.S. Pat. No. 5,752,011, the disclosure of both of which are incorporated herein by reference.

INT-CL: [07] G06 F 1/32, G06 F 1/08

US-CL-ISSUED: 713/322; 713/501
US-CL-CURRENT: 713/322; 713/501

FIELD-OF-SEARCH: 713/501, 715/320, 715/322, 715/500, 715/501

PRIOR-ART-DISCLOSED:

U.S. PATENT DOCUMENTS

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	PAT-NO	ISSUE-DATE	PATENTEE-NAME	US-CL
☐	3453601	July 1969	Bogert et al.	
☐	3941989	March 1976	McLaughlin et al.	
☐	4279020	July 1981	Christian et al.	
☐	4293927	October 1981	Hoshii	

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☐	4381552	April 1983	Nocilini et al.
☐	4409665	October 1983	Tubbs
☐	4448543	May 1984	Vail
☐	4670837	June 1987	Sheets
☐	4672228	June 1987	Swoboda
☐	4686386	August 1987	Tadao
☐	4689659	August 1987	Watanabe
☐	4698748	October 1987	Juzswik et al.
☐	4722669	February 1988	Kundert
☐	4734871	March 1988	Tsunoda et al.
☐	4756473	July 1988	Takemae et al.
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☐	4893271	January 1990	Davis et al.
☐	4924112	May 1990	Anderson et al.
☐	4970497	November 1990	Broadwater et al.
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☐	5021679	June 1991	Fairbanks et al.
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0 566 395	October 1993	EP
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58-099821	June 1983	JP
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"Computerized Control of Chilled Water System," IBM Technical Disclosure Bulletin, vol. 20, No. 8, pp. 2981-2984, Jan. 1978.
"Variable Air Cooling for Computer And/Or Electronic Equipment," IBM Technical Disclosure Bulletin, vol. 32, No. 10A, pp. 196-198, Mar. 1990.
Advanced Power Management (APM), BIOS Interface Specification, Revision 1.1, Sep. 1993.

ART-UNIT: 2185

PRIMARY-EXAMINER: Heckler; Thomas M.

ABSTRACT:

Improved approaches to providing thermal and power management for a computing device are disclosed. These approaches facilitate intelligent control of a processor's clock frequency and/or a fan's speed so as to provide thermal and/or power management for the computing device.

52 Claims, 10 Drawing figures

First Hit Fwd Refs

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L2: Entry 6 of 12 File: USPT Feb 9, 1999

DOCUMENT-IDENTIFIER: US 5870545 A
TITLE: System and method for performing flexible workflow process compensation in a distributed workflow management system

Detailed Description Text (31):
To monitor the progress of running process activities and support system management, the HP OpenPM engine 20 maintains a comprehensive log of all events using a log manager 70 and provides a native interface 79a as well as an SNMP 79b and CMIP 79c gateways to facilitate integration with the HP OpenView environment. The formats and contents of the logged information can be customized to support specific application needs.

Detailed Description Text (158):
The major advantage of using activities to compensate or cancel activities is flexibility. For example, the process designer 22a can design complex activities to compensate a process activity. Cancelation of compensation activities can also be readily supported. Finally, separating definition from use increases reusability. An activity, once defined, can be repeatedly used and possibly for different business purposes.

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L2: Entry 6 of 12 File: USPT Feb 9, 1999

DOCUMENT-IDENTIFIER: US 5870545 A
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L2: Entry 6 of 12 File: USPT Feb 9, 1999

US-PAT-NO: 5870545
DOCUMENT-IDENTIFIER: US 5870545 A

TITLE: System and method for performing flexible workflow process compensation in a distributed workflow management system

DATE-ISSUED: February 9, 1999

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Davis; James W.	Sunnyvale	CA		
Du; Weimin	San Jose	CA		
Shan; Ming-Chien	Saratoga	CA		

ASSIGNEE-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY	TYPE CODE
Hewlett-Packard Company	Palo Alto	CA			02

APPL-NO: 08/ 825853 [PALM]
DATE FILED: April 4, 1997

PARENT-CASE:
CROSS-REFERENCE TO RELATED APPLICATION This patent application is a continuation application of provisional application Ser. No. 60/032,567, filed on Dec. 5, 1996, by Weimin Du et. al., and entitled WORKFLOW/PROCESS FLOW PROCESS MANAGEMENT SYSTEM, the disclosure of which is incorporated herein by reference.

INT-CL: [06] G06 F 9/00

US-CL-ISSUED: 395/200.31
US-CL-CURRENT: 709/201

FIELD-OF-SEARCH: 364/DIG.1, 364/DIG.2, 395/180, 395/181, 395/182.01, 395/182.02, 395/182.03, 395/182.1, 395/183.2, 395/184.01, 395/200.3, 395/200.31-200.51, 395/670, 395/675, 707/103

PRIOR-ART-DISCLOSED:

U.S. PATENT DOCUMENTS

Search Selected Search ALL Clear

	PAT-NO	ISSUE-DATE	PATENTEE-NAME	US-CL
☐	5634127	May 1997	Cloud et al.	395/680

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☐	5745901	April 1998	Entner et al.	707/103

ART-UNIT: 278

PRIMARY-EXAMINER: Harrell; Robert B.

ABSTRACT:

A system and method for performing flexible workflow process compensation in a distributed workflow management system is described. A computer network includes a plurality of interconnected computers. Each computer includes a processor, memory and input/output facilities. The distributed workflow management system operates over the computer network. A plurality of resources perform the workflow process is performed with each resource operatively coupled to at least one of the computers. A process definition diagram includes computer-readable instructions stored in the memory of at least one of the computers and contains a role specification of process activities for performing the workflow process. A resource manager maps the role specification of process activities to at least one of the resources at runtime. A workflow process engine executes each process activity using the mapped resource and compensates a failed process activity responsive to the process definition diagram.

33 Claims, 18 Drawing figures

First Hit Fwd Refs

Generate Collection Print

L2: Entry 6 of 12 File: USPT Feb 9, 1999

US-PAT-NO: 5870545
DOCUMENT-IDENTIFIER: US 5870545 A

TITLE: System and method for performing flexible workflow process compensation in a distributed workflow management system

DATE-ISSUED: February 9, 1999

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Davis; James W.	Sunnyvale	CA		
Du; Weimin	San Jose	CA		
Shan; Ming-Chien	Saratoga	CA		

ASSIGNEE-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY	TYPE CODE
Hewlett-Packard Company	Palo Alto	CA			02

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INT-CL: [06] G06 F 9/00

US-CL-ISSUED: 395/200.31
US-CL-CURRENT: 709/201

FIELD-OF-SEARCH: 364/DIG.1, 364/DIG.2, 395/180, 395/181, 395/182.01, 395/182.02, 395/182.03, 395/182.1, 395/183.2, 395/184.01, 395/200.3, 395/200.31-200.51, 395/670, 395/675, 707/103

PRIOR-ART-DISCLOSED:

U.S. PATENT DOCUMENTS

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	PAT-NO	ISSUE-DATE	PATENTEE-NAME	US-CL
☐	5634127	May 1997	Cloud et al.	395/680

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☐	5745901	April 1998	Entner et al.	707/103

ART-UNIT: 278

PRIMARY-EXAMINER: Harrell; Robert B.

ABSTRACT:

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33 Claims, 18 Drawing figures

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First Hit Fwd Refs

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L2: Entry 8 of 12 File: USPT May 26, 1998

DOCUMENT-IDENTIFIER: US 5757640 A
TITLE: Product application control with distributed process manager for use on vehicles

Abstract Text (1):
A product application control system having at least one distributed network. Each distributed network includes at least one independent control module for controlling at least one activator device. The system includes a central processor which has a process distribution controller which monitors the level of processing activity of the central processor. The responsibility for processing objects is maintained in the central processor so long as the level of processing activity in the central processor does not exceed a predetermined target level. If the target level is exceeded the process distribution controller causes responsibility for processing one or more objects to be downloaded to at least one independent control module.

Brief Summary Text (23):
In one embodiment the invention is a mobile product application control system which includes a vehicle and at least one distributed network coupled to the vehicle. The distributed network includes at least one independent control module located at a node within the distributed network and having independent processing capability. The intelligent control module controls at least one actuator device in response to control setpoints generated from objects processed within the control system. The actuators are controlled in a manner that causes at least one predetermined product to be applied to a predetermined geographic land area at variable rates determined by the control setpoints. The system includes a central processor coupled to the at least one distributed network. The central processor has a process distribution controller which monitors the level of processing activity of the central processor. It is the process distribution controller which determines whether objects are processed within the central processor or the independent control modules. The responsibility for processing objects in maintained within the central processor so long as the level of processing activity in the central processor does not exceed a predetermined target level. If that predetermined target level is exceeded the process distribution controller causes the responsibility for processing one or more objects to be downloaded to at least one independent control module. The objects are downloaded based upon a predetermined priority level. Preferably, objects with the lowest priority are downloaded first. The system further includes at least one data input device coupled to either the distributed network or the central processor. The data in used in processing the objects.

Detailed Description Text (40):
As the size of the control system and the number of nodes and independent networks increases a greater burden is placed upon the host CPU. The size of the system thus dictates that at a certain level the host CPU will exceed its processing capacity and the system will slow down. This could result in delayed control, inaccurate control or even system failure. Recognizing the potential for this problem the present system utilizes a process manager. It is the function of the process manager to monitor the level of processing activity of the host CPU. When the host processing activity exceeds a certain predetermined target level, for example, 30%,

the process manager begins to download processing responsibility to the nodes based upon predetermined process priorities. Thus, the processing activity of the host CPU is maintained at or below a desired target level which allows sufficient capacity to free up the host to handle the multitude of communications which are required between different parts of the system in an efficient and timely manner.

CLAIMS:

1. A mobile product application control system comprising:

a vehicle;

at least one distributed network coupled to the vehicle, the at least one distributed network including at least one independent control module having processing capability for controlling at least one actuator device in response to control setpoints generated from objects processed within the control system, such that at least one predetermined product is applied to a predetermined geographic land area at variable rates determined by the control setpoints;

a central processor coupled to the at least one distributed network, the central processor including a process distribution controller which monitors the level of processing activity of the central processor and is responsive thereto to maintain responsibility of processing objects in the central processor so long as the level of processing activity in the central processor does not exceed a predetermined target level and to download responsibility for processing at least one object to at least one independent control module when the level of processing activity in the central processor exceeds the predetermined target level; and

at least one data input device coupled to at least one of the distributed network and the central processor, input data from the at least one data input device being used in processing at least one object.

8. A mobile product application control system comprising:

a vehicle;

at least one actuator device coupled to the vehicle;

independent processing and control means for controlling at least one actuator device in response to control setpoints generated from objects processed within the control system, such that at least one predetermined product is applied to a predetermined geographic land area at variable rates determined by the control setpoints;

at least one network means for distributing the independent processing and control means on a distributed network;

central processing means coupled to the at least one distributed network means, the central processing means including process distribution means for monitoring the level of processing activity within the central processing means and being responsive thereto to maintain responsibility for processing objects in the central processing means so long as the level of processing activity in the central processing means does not exceed a predetermined target level and to download the responsibility for processing at least one object to at least one independent processing and control means when the level of processing activity in the central processing means exceeds the predetermined target level; and

data input means for inputting data used in processing at least one object.

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L2: Entry 8 of 12 File: USPT May 26, 1998

US-PAT-NO: 5757640
DOCUMENT-IDENTIFIER: US 5757640 A

TITLE: Product application control with distributed process manager for use on vehicles

DATE-ISSUED: May 26, 1998

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Monson; Robert J.	St. Paul	MN		

ASSIGNEE-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY	TYPE CODE
Ag-Chem Equipment Co., Inc.	Minnetonka	MN			02

APPL-NO: 08/ 590933 [PALM]
DATE FILED: January 24, 1996

INT-CL: [06] G05 B 15/00

US-CL-ISSUED: 364/131; 364/138, 701/50, 701/1
US-CL-CURRENT: 700/2; 701/1, 701/50

FIELD-OF-SEARCH: 364/131-139, 364/423.098, 364/424.034, 364/424.036, 364/424.038, 364/424.04, 364/424.07, 111/922, 172/315, 180/900, 395/904, 395/905

PRIOR-ART-DISCLOSED:

U.S. PATENT DOCUMENTS

Search Selected Search ALL Clear

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☐	4176395	November 1979	Evelyn-Veere et al.	364/420
☐	4209131	June 1980	Barash et al.	239/68
☐	4277022	July 1981	Holdsworth et al.	239/7
☐	4350293	September 1982	Lestradet	239/155
☐	4392611	July 1983	Bachman et al.	239/74
☐	4527353	July 1985	Newby	47/59

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☐	4545396	October 1985	Miller et al.	137/78.3
☐	4553702	November 1985	Coffee et al.	239/690
☐	4588127	May 1986	Ehrat	239/156
☐	4630773	December 1986	Ortlip	239/1
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☐	4803626	February 1989	Bachman et al.	364/424.07
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☐	5220876	June 1993	Monson et al.	111/130
☐	5246164	September 1993	McCann et al.	239/11
☐	5260875	November 1993	Tofte et al.	364/424.07
☐	5313578	May 1994	Handorf	395/200
☐	5355815	October 1994	Monson	111/200
☐	5453924	September 1995	Monson et al.	364/131
☐	5463735	October 1995	Pascucci et al.	395/200.1

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"Data Transfer Bottlenecks over SPARC-Based Computer Networks", by E. Saulnier and B. Bortscheller, IEEE Local Computer Networks, 1995 20th Conference, pp. 289-295.
"An Efficient Recovery Protocol for Distributed Network Planning Information with Network Partitoning and Equipment Failure", by Farnham et al., Globecom '95 Communications for Global Harmony, IEEE Global Telecommunications, May 1995, pp. 952-957.

ART-UNIT: 234

PRIMARY-EXAMINER: Louis-Jacques; Jacques H.

ASSISTANT-EXAMINER: Frejd; Russell W.

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ABSTRACT:

A product application control system having at least one distributed network. Each distributed network includes at least one independent control module for controlling at least one activator device. The system includes a central processor which has a process distribution controller which monitors the level of processing activity of the central processor. The responsibility for processing objects is maintained in the central processor so long as the level of processing activity in the central processor does not exceed a predetermined target level. If the target level is exceeded the process distribution controller causes responsibility for processing one or more objects to be downloaded to at least one independent control module.

15 Claims, 14 Drawing figures

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Refine Search

Search Results -

Terms	Documents
L1 and ((increas$3 or decreas$3) same activity)	47

Database:

US Pre-Grant Publication Full-Text Database
US Patents Full-Text Database
US OCR Full-Text Database
EPO Abstracts Database
JPO Abstracts Database
Derwent World Patents Index
IBM Technical Disclosure Bulletins

Search: L4

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Search History

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L4	L1 and ((increas$3 or decreas$3) same activity)	47	L4
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L3	L2	0	L3
DB=USPT; PLUR=YES; OP=OR			
L2	L1 and ((increas$3 or decreas$3) same (process$3 adj1 activity))	12	L2
L1	monitor$3 near10 (process$3 adj1 activity)	142	L1

END OF SEARCH HISTORY

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Refine Search

Search Results -

Terms	Documents
L1 and ((increas$3 or decreas$3) same activity)	47

Database:

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US Patents Full-Text Database
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JPO Abstracts Database
Derwent World Patents Index
IBM Technical Disclosure Bulletins

Search: L4

Refine Search

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Search History

DATE: Wednesday, May 12, 2004 Printable Copy Create Case

Set Name side by side	Query	Hit Count	Set Name result set
	DB=USPT; PLUR=YES; OP=OR		
L4	L1 and ((increas$3 or decreas$3) same activity)	47	L4
	DB=EPAB,JPAB,DWPI,TDBD; PLUR=YES; OP=OR		
L3	L2	0	L3
	DB=USPT; PLUR=YES; OP=OR		
L2	L1 and ((increas$3 or decreas$3) same (process$3 adj1 activity))	12	L2
L1	monitor$3 near10 (process$3 adj1 activity)	142	L1

END OF SEARCH HISTORY

h e b b cg b e e ch

Refine Search

Search Results -

Terms	Documents
L4	0

Database:
US Pre-Grant Publication Full-Text Database
US Patents Full-Text Database
US OCR Full-Text Database
EPO Abstracts Database
JPO Abstracts Database
Derwent World Patents Index
IBM Technical Disclosure Bulletins

Search: L5

Refine Search

Recall Text | Clear | Interrupt

Search History

DATE: Wednesday, May 12, 2004 Printable Copy Create Case

Set Name side by side	Query	Hit Count	Set Name result set
DB=EPAB,JPAB,DWPI,TDBD; PLUR=YES; OP=OR			
L5	L4	0	L5
DB=USPT; PLUR=YES; OP=OR			
L4	L1 and ((increas$3 or decreas$3) same activity)	47	L4
DB=EPAB,JPAB,DWPI,TDBD; PLUR=YES; OP=OR			
L3	L2	0	L3
DB=USPT; PLUR=YES; OP=OR			
L2	L1 and ((increas$3 or decreas$3) same (process$3 adj1 activity))	12	L2
L1	monitor$3 near10 (process$3 adj1 activity)	142	L1

END OF SEARCH HISTORY

h e b b cg b e e ch

L4: Entry 46 of 47 File: USPT Feb 23, 1988

DOCUMENT-IDENTIFIER: US 4727549 A
**** See image for Certificate of Correction ****
TITLE: Watchdog activity monitor (WAM) for use wth high coverage processor self-test

Abstract Text (1):
A high fault coverage, instruction modeled self-test for a signal processor in a user environment is disclosed. The self-test executes a sequence of sub-tests and issues a state transition signal upon the execution of each sub-test. The self-test may be combined with a watchdog activity monitor (WAM) which provides a test-failure signal in the presence of a counted number of state transitions not agreeing with an expected number. An independent measure of time may be provided in the WAM to increase fault coverage by checking the processor's clock. Additionally, redundant processor systems are protected from inadvertent unsevering of a severed processor using a unique unsever arming technique and apparatus.

Brief Summary Text (13):
It is essential, in order to understand the central teaching of this first aspect of the present invention, to understand that the timing aspects of the WDTs of the prior art have been abandoned in the WAM of the present invention. The processor self-test is set-up in advance to test the major functional blocks of the signal processor. These may include bit manipulation tests, logical operation tests, addition and subtraction operational tests, divide and multiply operational tests, and rotate and shift operational tests. Of course, a variety of these tests may be excluded and other tests may be included. At the conclusion of each of the above major categories of tests a transition is made to the next major category of tests. At that time, a transition signal is sent into the Watchdog Activity Monitor indicating that one of the major tests has been completed. Of course, transition signals could be sent more frequently, at the conclusion of minor test steps accomplished within each major functional test block. Each time that the WAM receives a transition signal it increases or decreases a count signal magnitude which keeps track of the total number of state transitions which have taken place for each repetition of the periodic test. At the conclusion of each repetition of the test a reset signal is sent by the CPU to the WAM. If the reset signal arrives at the WAM while the count signal magnitude is equal to an expected magnitude then the WAM will have ascertained that a correct number of test executions have taken place and a channel sever signal will not be issued.

Brief Summary Text (17):
The Watchdog Activity Monitor and self-test method of the present invention provides an attractive alternative to prior art methods and apparatus for detecting faults in signal processors in a user environment. By marrying a unique self-test method based on the processor subfunctions with a unique Watchdog Activity Monitor, a very high degree of failure coverage is achieved. Furthermore, the use of a second keep-alive "ticket-punch" type timer for guaranteeing the health of the system clock, the present invention further increases its failure coverage.

Detailed Description Text (15):
The self-test begins in a start step 100. During the execution of each test the processor activity signals are monitored by the WAM to count up or down the number

of steps executed. At the end of the sequence a ticket-punch or reset is sent, as indicated in a step 102, to the WAM hardware. If the WAM hardware does not receive the ticket-punch signal precisely when the count reaches a selected total count or count-down, a channel sever is immediately executed by the WAM hardware. After successful execution the above test procedure may then be reexecuted periodically after returning in a step 103 and starting again at step 100.

First Hit Fwd Refs

Generate Collection Print

L4: Entry 46 of 47 File: USPT Feb 23, 1988

US-PAT-NO: 4727549
DOCUMENT-IDENTIFIER: US 4727549 A
**** See image for Certificate of Correction ****

TITLE: Watchdog activity monitor (WAM) for use wth high coverage processor self-test

DATE-ISSUED: February 23, 1988

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Tulpule; Bhalchandra R.	Vernon	CT		
Crosset, III; Richard W.	Simsbury	CT		
Versailles; Richard E.	New Hartford	CT		

ASSIGNEE-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY	TYPE CODE
United Technologies Corporation	Hartford	CT			02

APPL-NO: 06/ 758251 [PALM]
DATE FILED: September 13, 1985

INT-CL: [04] G06F 11/00

US-CL-ISSUED: 371/62; 371/25
US-CL-CURRENT: 714/55; 714/736

FIELD-OF-SEARCH: 371/15, 371/25, 371/62, 324/73R, 324/73AT, 324/73PC

PRIOR-ART-DISCLOSED:

U.S. PATENT DOCUMENTS

Search Selected Search ALL Clear

	PAT-NO	ISSUE-DATE	PATENTEE-NAME	US-CL
☐	3749897	July 1973	Hirvela	371/62 X
☐	3919637	November 1975	Earp	371/25
☐	4161276	July 1979	Sacher et al.	371/25
☐	4176780	December 1979	Sacher et al.	371/25
☐	4392226	July 1983	Cook	371/61
☐	4410938	October 1983	Higashiyama	371/62 X

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☐	4594685	June 1986	Owens	371/62 X
☐	4635258	January 1987	Salowe	371/62 X

OTHER PUBLICATIONS

J. P. Hayes, Transition Count Testing of Combinational Logic Circuits, IEEE Trans. on Computers, vol. C-25, No. 6, Jun. 1976, pp. 613-620.

ART-UNIT: 236

PRIMARY-EXAMINER: Atkinson; Charles E.

ATTY-AGENT-FIRM: Maguire, Jr.; Francis J.

ABSTRACT:

A high fault coverage, instruction modeled self-test for a signal processor in a user environment is disclosed. The self-test executes a sequence of sub-tests and issues a state transition signal upon the execution of each sub-test. The self-test may be combined with a watchdog activity monitor (WAM) which provides a test-failure signal in the presence of a counted number of state transitions not agreeing with an expected number. An independent measure of time may be provided in the WAM to increase fault coverage by checking the processor's clock. Additionally, redundant processor systems are protected from inadvertent unsevering of a severed processor using a unique unsever arming technique and apparatus.

13 Claims, 8 Drawing figures

First Hit Fwd Refs

Generate Collection Print

L4: Entry 46 of 47 File: USPT Feb 23, 1988

US-PAT-NO: 4727549
DOCUMENT-IDENTIFIER: US 4727549 A
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TITLE: Watchdog activity monitor (WAM) for use wth high coverage processor self-test

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Versailles; Richard E.	New Hartford	CT		

ASSIGNEE-INFORMATION:

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United Technologies Corporation	Hartford	CT			02

APPL-NO: 06/ 758251 [PALM]
DATE FILED: September 13, 1985

INT-CL: [04] G06F 11/00

US-CL-ISSUED: 371/62; 371/25
US-CL-CURRENT: 714/55; 714/736

FIELD-OF-SEARCH: 371/15, 371/25, 371/62, 324/73R, 324/73AT, 324/73PC

PRIOR-ART-DISCLOSED:

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	PAT-NO	ISSUE-DATE	PATENTEE-NAME	US-CL
☐	3749897	July 1973	Hirvela	371/62 X
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☐	4410938	October 1983	Higashiyama	371/62 X

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ART-UNIT: 236

PRIMARY-EXAMINER: Atkinson; Charles E.

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ABSTRACT:

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13 Claims, 8 Drawing figures

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L4: Entry 46 of 47 File: USPT Feb 23, 1988

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TITLE: Watchdog activity monitor (WAM) for use wth high coverage processor self-test

DATE-ISSUED: February 23, 1988

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ART-UNIT: 236

PRIMARY-EXAMINER: Atkinson; Charles E.

ATTY-AGENT-FIRM: Maguire, Jr.; Francis J.

ABSTRACT:

A high fault coverage, instruction modeled self-test for a signal processor in a user environment is disclosed. The self-test executes a sequence of sub-tests and issues a state transition signal upon the execution of each sub-test. The self-test may be combined with a watchdog activity monitor (WAM) which provides a test-failure signal in the presence of a counted number of state transitions not agreeing with an expected number. An independent measure of time may be provided in the WAM to increase fault coverage by checking the processor's clock. Additionally, redundant processor systems are protected from inadvertent unsevering of a severed processor using a unique unsever arming technique and apparatus.

13 Claims, 8 Drawing figures

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First Hit Fwd Refs

Generate Collection Print

L4: Entry 44 of 47 File: USPT Sep 25, 1990

DOCUMENT-IDENTIFIER: US 4959782 A
TITLE: Access arbitration for an input-output controller

Abstract Text (1):
Arbitration access to an IOC's RAM between the IOC's I/O bus and a signal processor is accomplished by always granting the signal processor access to the IOC's RAM for one machine cycle and disallowing any signal processor operations which would otherwise permit preemptive demand access to memory for more than one machine cycle. The signal processor's activity is then monitored for detecting the signal processor engaged in an activity which does not presently require access to the IOC's RAM and which will occupy the signal processor in a non-memory access activity for a predictable period of time. The IOC's I/O bus is then granted access to the IOC's RAM for a period of time less than the predicted period. In addition to this transparency feature, the present invention may be used in a context of a unique method of transferring data between sensors and actuators on one side of the IOC and the signal processor on the other side. This may be done either according to a default sequence or any one of a plurality of selectable modes of data transfer sequences. The present invention may additionally be used in a redundant channel system for communicating input-output data between channels in blocks in a predefined protocol in which data is transmitted between each channel and all of the channels over cross-channel data links. The blocks are deposited in a portion of link memory partitioned according to the source channel.

Brief Summary Text (16):
The gathering and distribution of data by any IOC requires access to memory which is also being used by the control processor. This is most commonly done in a direct memory access (DMA) mode where the processor is requested access to the data/address buses and the data is transferred on receipt of a bus grant signal. During this transfer interval, the processor is essentially idle. This loss of real time by the processor linearly increases with the number of data transfers by the IOC, to a point where it can significantly affect the overall throughput capability of the host processor. Another difficulty with this DMA approach is that the bus grant signal is essentially asynchronous and may take more or less time depending upon the processor and its current activity. If the bus grant signal is held off for a long time, it can lead to loss of rapidly arriving internal bus messages, particularly if they are asynchronous in nature. A common solution to this problem is to buffer the incoming bus data. However, this approach has a significant hardware penalty and can only provide limited relief. Another, new approach, disclosed herein, involves the use of dual port RAMs which can internally arbitrate between two asynchronous data buses for memory accesses. However, this also has a significant hardware penalty and, though it fulfills the need for an autonomous bus between the IOC and the control processor's memory, it is not always affordable.

Brief Summary Text (23):
More specifically, the method for arbitrating access to an IOC's RAM (non-dual-port) as between the IOC's I/O bus and a signal processor, comprises the steps of (1) always granting the signal processor access to the IOC's RAM upon receipt of a demand for the RAM for one machine cycle by the signal processor; (2) inhibiting the CPU from preemptively demanding access to memory for more than one machine cycle; (3) monitoring the signal processor's activity to detect the signal

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processor engaged in an activity which does not require access to the IOC's RAM and which will certainly occupy the signal processor in a non-memory access activity for a known period of time; and (4) using the known period of time to permit the IOC's I/O bus to gain access to the IOC's RAM for less than the known period.

CLAIMS:

1. A method for arbitrating access to an input-output controller's (IOC's) random access memory (RAM) between the IOC's input-output (I/O) bus and a signal processor's I/O bus, the IOC's I/O bus being connected to a plurality of sensors and actuators, the signal processor having an instruction set, each instruction requiring one or more minimum machine cycles for execution, comprising the steps of:

having the IOC always grants the signal processor access to the IOC's RAM upon receipt of a demand by the signal processor for access to the IOC's RAM;

having the IOC monitor the signal processor's activity at the beginning of each machine cycle to detect the signal processor engaged in an activity which does not require access to the IOC's RAM and in which it will be engaged in a non-IOC RAM access activity for the minimum machine cycle; and

having the IOC, upon detecting the processor so engaged, permit the IOC's I/O bus to gain access to the IOC's RAM, but only during the minimum machine cycle.

3. An input-output controller (IOC) for transferring data between a signal processor which provides selected signals indicative of the activity it will perform in a current machine cycle, and devices external to both the IOC and the processor via an IOC random access memory (RAM), comprising:

arbitration means for always providing a grant signal to the signal processor for granting the signal processor access to the IOC's RAM in response to a demand signal from the signal processor for access to the IOC's RAM, said arbitration means also responsive to the selected signals from the signal processor for monitoring the signal processor's activity in order to detect when the signal processor is engaged in an activity which does not require access to the IOC's RAM and which will engage the signal processor in a non-IOC RAM access activity for at least one machine cycle; and

means for permitting the IOC's I/O bus to gain access to the IOC's RAM, for each machine cycle during which the processor is detected as being engaged in non-IOC RAM access activities.

4. A method for communicating input-output data between a plurality of similar input-output controllers (IOCs) each having a related one of a like plurality of similar signal processors associated therewith, and for arbitrating access to each IOC's random access memory (RAM) between such IOC's input-output (I/O) bus and the I/O bus of the related signal processor, each IOC's I/O bus being connected to a plurality of sensors and actuators, each signal processor having an instruction set of which each instruction requires at least one minimum machine cycle for execution, comprising the steps of:

having each IOC always grant the related signal process access to such IOC's RAM upon receipt of a demand by the related signal processor for access to such IOC's RAM;

having each IOC monitor the related signal processor's activity at the beginning of each machine cycle to detect when the related signal processor is engaged in an activity which does not require access to such IOC's RAM and in which such related signal processor will be engaged in a non-IOC RAM access activity for the minimum

machine cycle;

having each IOC, upon detecting that the related signal processor is so engaged, permit such IOC's I/O bus to gain access to such IOC's RAM, but only during the minimum machine cycle;

having each IOC format data words in blocks having an IOC identifier for transmission to the other IOCs;

having each IOC transmit formatted data blocks to all of the other IOCs;

having each IOC receive data blocks transmitted from each of the other IOCs;

having each IOC generate, for each word received by it, a memory address corresponding to the IOC from which the associated block originated; and

having each IOC store each word received by such IOC at the memory address generated by such IOC.

5. A method for communicating input-output data between a plurality of similar input-output controllers (IOCs) each having a related one of a like plurality of similar signal processors associated therewith, and for arbitrating access to each IOC's random access memory (RAM) between such IOC's input-output (I/O) bus and the I/O bus of the related signal processor, each IOC's I/O bus being connected to a plurality of sensors and actuators, each signal processor having an instruction set of which each instruction requires at least one minimum machine cycle for execution, comprising the steps of:

having each IOC always grant the related signal processor access to such IOC's RAM upon receipt of a demand by the related signal processor for access to such IOC's RAM;

having each IOC monitor the related signal processor's activity at the beginning of each machine cycle to detect when the related signal processor is engaged in an activity which does not require access to such IOC's RAM and in which such related signal processor will be engaged in a non-IOC RAM access activity for the minimum machine cycle;

having each IOC, upon detecting that the related signal processor is so engaged, permit such IOC's I/O bus to gain access to such IOC's RAM, but only during the minimum machine cycle;

having each IOC format data in blocks for transmission to the other IOCs, each block having an initial command word having a command word identifier protocol followed by an origination code and a starting address, the command word followed by a variable number of other words, the first other word having a data word identifier protocol followed by a word count, the second and remaining other words each having a data word identifier protocol followed by data words;

having each IOC transmit blocks formatted by it to the other IOCs;

having each IOC receive the blocks transmitted from other IOCs;

having each IOC store received blocks according to the identity of the transmitting IOC and the starting address in the next available sequential memory location after the end of the previously received block;

having each IOC generate, for each block received by it, a stop address according to the start address plus the word count; and

having each IOC store the stop address of each block received by it at the start address and store subsequently received data words of such block sequentially after the start address.

6. A system including a plurality of input-output controllers (IOCs), each for communicating input-output data between itself and other ones of said IOCs, and each for transferring data between a related one of a like plurality of signal processors associated with said IOC and provides selected signals indicative of the activity it will perform in a current machine cycle, and devices external to both said IOC and its related processor via a related one of a like plurality of IOC random access memories (RAMs), each IOC comprising:

arbitration means for always providing a grant signal to the related signal processor for granting such signal processor access to said IOC's RAM in response to a demand signal from such signal processor for access to the IOC's RAM, said arbitration means also responsive to the selected signals from the related signal processor for monitoring such signal processor's activity in order to detect when such signal processor is engaged in an activity which does not require access to said IOC's RAM and which will engage such signal processor in a non-IOC RAm access activity for at least one machine cycle;

means for permitting said IOC's I/O bus to gain access to said IOC's RAM, for each machine cycle during which the related processor is detected as being engaged in non-IOC RAM access activities;

means for formatting data words in blocks for transmission to said other IOCs;

means for transmitting formatted data blocks to said other iOCs;

means for receiving the data blocks transmitted from each other IOC;

means for generating, for each word received by said IOC, a memory address corresponding to the IOC from which the associated block originated; and

means for storing each word received by said IOC at the memory address generated by said IOC.

7. A system including a plurality of input-output controllers (IOCs), each for communicating input-output data between itself and other ones of said IOCs, and each for transferring data between a related one of a like plurality of signal processors associated with said IOC and provides selected signals indicative of the activity it will perform in a current machine cycle, and devices external to both said IOC and its related processor via a related one of a like plurality of IOC random access memories (RAMs), each IOC comprising:

arbitration means for always providing a grant signal to the related signal processor for granting such signal processor access to said IOC's RAM in response to a demand signal from such signal processor for access to the IOC's RAM, said arbitration means also responsive to the selected signals from the related signal processor for monitoring such signal processor's activity in order to detect when such signal processor is engage din an activity which does not require access to said IOC's RAM and which will engage such signal processor in a non-IOC RAM access activity for at least one machine cycle;

means for permitting said IOC's I/O bus to gain access to said IOC's RAM, for each machine cycle during which the related processor is detected as being engaged in non-IOC RAM access activities;

means for formatting data words for transmission in blocks, each block having an initial command word having a command word identifier protocol followed by an

origination code and a starting address, the command word followed by a variable number of other words, the first other word having a data word identifier protocol followed by a word count, the second and remaining other words each having a data word identifier protocol followed by data words;

means for transmitting blocks formatted by said IOC to all of the other IOCs;

means for receiving the blocks transmitted form other IOCs; and

means for storing blocks received by said IOC according to the identity of the transmitting IOC by storing the starting address in the next available sequential memory location after the end of the previously received block, generating a stop address according to the start address plus the word count, and storing subsequently received data words of such block sequentially after the start address.

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L4: Entry 44 of 47 File: USPT Sep 25, 1990

US-PAT-NO: 4959782
DOCUMENT-IDENTIFIER: US 4959782 A

TITLE: Access arbitration for an input-output controller

DATE-ISSUED: September 25, 1990

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Tulpule; Bhalchandra R.	Vernon	CT		
Binnall; Daniel G.	Simsbury	CT		

ASSIGNEE-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY	TYPE CODE
United Technologies Corporation	Hartford	CT			02

APPL-NO: 07/ 465590 [PALM]
DATE FILED: January 18, 1990

PARENT-CASE:
This is a continuation of application Ser. No. 06/924,647, filed Oct. 29, 1986, now abandoned.

INT-CL: [05] G06F 13/28, G06F 13/00

US-CL-ISSUED: 364/200; 364/900
US-CL-CURRENT: 710/240

FIELD-OF-SEARCH: 364/200, 364/900

PRIOR-ART-DISCLOSED:

U.S. PATENT DOCUMENTS

Search Selected Search ALL Clear

	PAT-NO	ISSUE-DATE	PATENTEE-NAME	US-CL
☐	4309754	January 1982	Dinwiddie, Jr.	364/200
☐	4514808	April 1985	Murayama et al.	364/200
☐	4543629	September 1985	Carey et al.	364/200
☐	4558412	December 1985	Inoshita et al.	364/200
☐	4604683	August 1986	Russ et al.	364/200

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☐	4665482	May 1987	Murray, Jr. et al.	364/200
☐	4675803	June 1987	Kendall et al.	364/200
☐	4688166	August 1987	Schneider	364/200
☐	4695952	September 1987	Howland	364/200
☐	4716523	December 1987	Burrus, Jr. et al.	364/200
☐	4750113	June 1988	Buggert	364/200

FOREIGN PATENT DOCUMENTS

FOREIGN-PAT-NO	PUBN-DATE	COUNTRY	US-CL
0204960	December 1986	EP	364/200

ART-UNIT: 253

PRIMARY-EXAMINER: James; Andrew J.

ASSISTANT-EXAMINER: Nguyen; Viet Q.

ATTY-AGENT-FIRM: Maguire, Jr.; Francis J.

ABSTRACT:

Arbitration access to an IOC's RAM between the IOC's I/O bus and a signal processor is accomplished by always granting the signal processor access to the IOC's RAM for one machine cycle and disallowing any signal processor operations which would otherwise permit preemptive demand access to memory for more than one machine cycle. The signal processor's activity is then monitored for detecting the signal processor engaged in an activity which does not presently require access to the IOC's RAM and which will occupy the signal processor in a non-memory access activity for a predictable period of time. The IOC's I/O bus is then granted access to the IOC's RAM for a period of time less than the predicted period. In addition to this transparency feature, the present invention may be used in a context of a unique method of transferring data between sensors and actuators on one side of the IOC and the signal processor on the other side. This may be done either according to a default sequence or any one of a plurality of selectable modes of data transfer sequences. The present invention may additionally be used in a redundant channel system for communicating input-output data between channels in blocks in a predefined protocol in which data is transmitted between each channel and all of the channels over cross-channel data links. The blocks are deposited in a portion of link memory partitioned according to the source channel.

7 Claims, 9 Drawing figures

L4: Entry 42 of 47 File: USPT Mar 30, 1993

DOCUMENT-IDENTIFIER: US 5197489 A
TITLE: Activity monitoring apparatus with configurable filters

Brief Summary Text (23):
In particular, so that a low amplitude signal, such as those produced by breathing and heart beats, can be isolated for later processing, the activity monitor includes signal conditioning means in the form of a motion signal amplifier having an amplification factor selectable by an applied configuration control signal, and a highpass filter circuit having a threshold selectable by another applied configuration signal below which motion sensor signals are greatly attenuated. This is advantageous in that it allows observations to be made of a subject both during a high activity period, when a relatively high amplitude high frequency signal is produced by the sensor, and during a low activity period, such as during the night, when the subject is typically producing a relatively low amplitude and low frequency signal.

Detailed Description Text (55):
The dynamic range of human motion is large, typically in the order of 1000 to 1. For this reason it is critical that the gain of any amplifier used to sense analog motion be appropriately scaled. In the activity monitor of the present invention, the scaling is accomplished automatically by the monitor processor circuit 43. This ability is particularly useful where human activity is observed both during the day, when activity is greater, and at night, when activity usually decreases dramatically during sleep. The ability to schedule changes in gain according to the time of day allows the activity monitor of the present invention to optimize signal resolution and avoid signal saturation. This is also true of the ability to switch frequency bands.

Detailed Description Text (72):
However, frequency itself is not a sufficient criteria for separating and observing important activity It is desirable to utilize sensitivity to further discriminate and isolate motion of interest. For example, if a particular study involves determining the total number of minutes of sleep, it is not desirable to record heart rate or breathing which can be detected over the standard sleep band of 0.2 to 3 hertz. BY reducing amplifier gain and increasing the detection threshold, these two signals drop out, but bulk body and wrist motions do not. This is because the bulk motions create large amplitude signals easily detected by the detector circuitry. Similarly, daytime activity resides in the 0.2 to 3 hertz band but nighttime sensitivity is too high and will cause amplifier saturation and loss of higher energy daytime activity. Reduction of sensitivity overcomes this problem.

Detailed Description Text (88):
Option 2--Fixed Initialization--In this mode once the activity monitor is removed from the interface unit no changes to the operating parameters can occur, except for an AGC option wherein monitor gain is reduced or increased depending on the status of the saturation channel.

L4: Entry 42 of 47 File: USPT Mar 30, 1993

DOCUMENT-IDENTIFIER: US 5197489 A
TITLE: Activity monitoring apparatus with configurable filters

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However, frequency itself is not a sufficient criteria for separating and observing important activity It is desirable to utilize sensitivity to further discriminate and isolate motion of interest. For example, if a particular study involves determining the total number of minutes of sleep, it is not desirable to record heart rate or breathing which can be detected over the standard sleep band of 0.2 to 3 hertz. BY reducing amplifier gain and increasing the detection threshold, these two signals drop out, but bulk body and wrist motions do not. This is because the bulk motions create large amplitude signals easily detected by the detector circuitry. Similarly, daytime activity resides in the 0.2 to 3 hertz band but nighttime sensitivity is too high and will cause amplifier saturation and loss of higher energy daytime activity. Reduction of sensitivity overcomes this problem.

Detailed Description Text (88):
Option 2--Fixed Initialization--In this mode once the activity monitor is removed from the interface unit no changes to the operating parameters can occur, except for an AGC option wherein monitor gain is reduced or increased depending on the status of the saturation channel.

First Hit Fwd Refs

Generate Collection Print

L4: Entry 42 of 47 File: USPT Mar 30, 1993

US-PAT-NO: 5197489
DOCUMENT-IDENTIFIER: US 5197489 A

TITLE: Activity monitoring apparatus with configurable filters

DATE-ISSUED: March 30, 1993

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Conlan; Robert W.	Niceville	FL		

ASSIGNEE-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY	TYPE CODE
Precision Control Design, Inc.	Fort Walton Beach	FL			02

APPL-NO: 07/ 716853 [PALM]
DATE FILED: June 17, 1991

INT-CL: [05] A61B 5/103

US-CL-ISSUED: 128/782; 128/670, 128/671, 128/690, 128/721
US-CL-CURRENT: 600/595; 600/484, 600/503, 600/534

FIELD-OF-SEARCH: 128/782, 128/774, 128/690, 128/721, 128/722, 128/670, 128/671, 128/687, 128/713, 128/714, 128/419PG, 128/419PT, 340/573

PRIOR-ART-DISCLOSED:

U.S. PATENT DOCUMENTS

Search Selected Search ALL Clear

	PAT-NO	ISSUE-DATE	PATENTEE-NAME	US-CL
☐	3807388	April 1974	Orr et al.	128/690
☐	4088139	May 1978	Auerbach	128/419PT
☐	4117834	October 1978	McPartland et al.	128/782
☐	4202350	May 1980	Walton	128/690
☐	4353375	October 1982	Colburn et al.	128/782
☐	4425921	January 1984	Fujisaki et al.	128/690
☐	4428378	January 1984	Anderson et al.	128/419PG
☐	4819652	April 1989	Micco	128/661.09

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☐	4830021	May 1989	Thornton	128/707
☐	4945916	August 1990	Kretschmer et al.	128/671
☐	4989612	February 1991	Fore	128/721
☐	5010887	April 1991	Thornander	128/696
☐	5010893	April 1991	Sholder	128/782
☐	5025791	June 1991	Niwa	128/670
☐	5031614	July 1991	Alt	128/419OPG
☐	5036856	August 1991	Thornton	128/670
☐	5044365	September 1991	Webb et al.	128/419PG
☐	5074303	December 1991	Hauck	128/419PG

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Experimental Prototype (AM-16) Block Diagram.
Redmond, D. and Hegge, F., Observations on the design and specification of a wrist-worn human activity monitoring system Behavior Res. Methods, Instruments & Computer 1985 17(6), 659-669.

ART-UNIT: 339

PRIMARY-EXAMINER: Hindenburg; Max

ASSISTANT-EXAMINER: Tucker; Guy V.

ATTY-AGENT-FIRM: Lockwood, Alex, Fitzgibbon & Cummings

ABSTRACT:

An activity monitor adapted to be worn on the non-dominant wrist of a subject includes a bimorphous beam motion sensor. The output signal of the sensor is amplified in an amplifier circuit having a selectable amplification factor, and filtered by highpass and lowpass filter circuits having individually selectable cut-off frequencies to obtain an analog signal for processing having a bandpass and amplitude characteristic corresponding to a particular body activity under observation. A control and processing circuit within the monitor includes a microprocessor which responds to either resident internal operating instructions or to externally supplied operating instructions, or to designated data signal parameters, to provide configuration control signals to the amplifier and filter circuits, and processing of the collected data, appropriate to the particular activity being monitored. The processed data is digitally stored in an internal memory for subsequent transfer through a data port to an associated computer for display or further processing.

33 Claims, 18 Drawing figures

L4: Entry 38 of 47 File: USPT Jun 27, 1995

DOCUMENT-IDENTIFIER: US 5428806 A
**** See image for Certificate of Correction ****
TITLE: Computer networking system including central chassis with processor and input/output modules, remote transceivers, and communication links between the transceivers and input/output modules

Detailed Description Text (32):
The processor module 8 of FIGS. 1 and 5 is shown in block diagram form in FIGS. 12, 13A and 13B. The connection of the processor module 8 to the backplane 4 in the chassis 2 is provided through 144 pin male connector 17 and 48 pin male connector 18. The main processing portion of the processor module 8 includes a processor bus, such as an industry standard ISA bus 230, and a microprocessor 232, such as an Intel 80386 or 80486. The processor bus 230 could follow other industry standards, such as EISA or the like. Communication between the microprocessor 232 and the ISA bus 230 is controlled by a system controller 234. Extending between the microprocessor 232 and the system controller 234 are a control bus, address bus and data bus. These three bus lines can also extend to an optional numeric coprocessor 236 which, if used, helps to speed up the activities of the microprocessor 232. The address bus and data bus may also be supplied to an optional cache memory 238 which is used, under control of the system controller 234, to increase overall performance of the microprocessor 232. The system controller 234 transmits ISA DMA Acknowledge and ISA Control signals to the ISA bus 230. Likewise, the ISA bus transmits ISA DMA Request and ISA Interrupt Request signals to the system controller 234.

Detailed Description Text (55):
In all situations, control passes from block 404 to block 422 where the next I/O channel interface in a particular I/O module is selected and all of the steps discussed above, downstream of the start block 390, are repeated. In this manner, the I/O module continually monitors keyboard activity and processing activity through each of its I/O channel inferaces.

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L4: Entry 38 of 47 File: USPT Jun 27, 1995

US-PAT-NO: 5428806
DOCUMENT-IDENTIFIER: US 5428806 A
** See image for Certificate of Correction **

TITLE: Computer networking system including central chassis with processor and input/output modules, remote transceivers, and communication links between the transceivers and input/output modules

DATE-ISSUED: June 27, 1995

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Pocrass; Alan L.	Simi Valley	CA	93065	

APPL-NO: 08/ 008008 [PALM]
DATE FILED: January 22, 1993

INT-CL: [06] G06 F 15/00

US-CL-ISSUED: 395/800; 395/200, 364/242.94, 364/929.5, 364/931.4, 364/940.61, 364/DIG.2
US-CL-CURRENT: 710/104; 710/100

FIELD-OF-SEARCH: 395/800, 395/200, 395/275, 370/94.2, 370/95.2, 370/95.3, 370/85.6, 358/86, 364/242.94, 364/929.5, 364/931.4, 364/940.61, 364/DIG.2

PRIOR-ART-DISCLOSED:

U.S. PATENT DOCUMENTS

Search Selected Search ALL Clear

	PAT-NO	ISSUE-DATE	PATENTEE-NAME	US-CL
☐	4787031	November 1988	Karger et al.	395/800
☐	5058110	October 1991	Beach et al.	370/85.6
☐	5062059	October 1991	Youngblood et al.	395/275
☐	5113496	May 1992	McCalley et al.	395/200
☐	5124982	June 1992	Kaku	370/85.3
☐	5226120	July 1993	Brown et al.	395/200
☐	5274767	December 1993	Maskovyak	395/275

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ART-UNIT: 232

PRIMARY-EXAMINER: Bowler; Alyssa H.

ASSISTANT-EXAMINER: Harrity; John

ATTY-AGENT-FIRM: Webb Ziesenheim Bruening Logsdon Orkin & Hanson

ABSTRACT:

A computer networking system includes a plurality of computer processing modules and at least one I/O module connected together through a backplane in a chassis at a central location. Users at variou remote locations connect at least a keyboard and a monitor to a transceiver unit. A data communication link is established between each transceiver and a unit interface on an I/O module. Data flow between the processor modules and the transceivers, as well as an allocation of processing module resources, are controlled by the I/O modules. The processor modules are connected together through at least one high speed network bus in the backplane.

20 Claims, 20 Drawing figures

First Hit Fwd Refs

Generate Collection Print

L4: Entry 38 of 47 File: USPT Jun 27, 1995

US-PAT-NO: 5428806
DOCUMENT-IDENTIFIER: US 5428806 A
** See image for Certificate of Correction **

TITLE: Computer networking system including central chassis with processor and input/output modules, remote transceivers, and communication links between the transceivers and input/output modules

DATE-ISSUED: June 27, 1995

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Pocrass; Alan L.	Simi Valley	CA	93065	

APPL-NO: 08/ 008008 [PALM]
DATE FILED: January 22, 1993

INT-CL: [06] G06 F 15/00

US-CL-ISSUED: 395/800; 395/200, 364/242.94, 364/929.5, 364/931.4, 364/940.61, 364/DIG.2
US-CL-CURRENT: 710/104; 710/100

FIELD-OF-SEARCH: 395/800, 395/200, 395/275, 370/94.2, 370/95.2, 370/95.3, 370/85.6, 358/86, 364/242.94, 364/929.5, 364/931.4, 364/940.61, 364/DIG.2

PRIOR-ART-DISCLOSED:

U.S. PATENT DOCUMENTS

Search Selected Search ALL Clear

	PAT-NO	ISSUE-DATE	PATENTEE-NAME	US-CL
☐	4787031	November 1988	Karger et al.	395/800
☐	5058110	October 1991	Beach et al.	370/85.6
☐	5062059	October 1991	Youngblood et al.	395/275
☐	5113496	May 1992	McCalley et al.	395/200
☐	5124982	June 1992	Kaku	370/85.3
☐	5226120	July 1993	Brown et al.	395/200
☐	5274767	December 1993	Maskovyak	395/275

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ART-UNIT: 232

PRIMARY-EXAMINER: Bowler; Alyssa H.

ASSISTANT-EXAMINER: Harrity; John

ATTY-AGENT-FIRM: Webb Ziesenheim Bruening Logsdon Orkin & Hanson

ABSTRACT:

A computer networking system includes a plurality of computer processing modules and at least one I/O module connected together through a backplane in a chassis at a central location. Users at variou remote locations connect at least a keyboard and a monitor to a transceiver unit. A data communication link is established between each transceiver and a unit interface on an I/O module. Data flow between the processor modules and the transceivers, as well as an allocation of processing module resources, are controlled by the I/O modules. The processor modules are connected together through at least one high speed network bus in the backplane.

20 Claims, 20 Drawing figures

First Hit Fwd Refs

Generate Collection Print

L4: Entry 22 of 47 File: USPT Jul 21, 1998

US-PAT-NO: 5784598
DOCUMENT-IDENTIFIER: US 5784598 A
**** See image for Certificate of Correction ****

TITLE: Method and apparatus for changing processor clock rate

DATE-ISSUED: July 21, 1998

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Griffith; Jenni L.	Belton	TX		

ASSIGNEE-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY	TYPE CODE
Texas Instruments Incorporated	Dallas	TX			02

APPL-NO: 08/ 479580 [PALM]
DATE FILED: June 7, 1995

PARENT-CASE:
This application is a Continuation of application Ser. No. 07/897,693 filed Jun. 12, 1992, now abandoned.

INT-CL: [06] G06 F 1/08

US-CL-ISSUED: 395/556; 395/560
US-CL-CURRENT: 713/501; 713/601

FIELD-OF-SEARCH: 395/550, 395/750, 395/555, 395/556, 395/559, 395/560, 395/750.04

PRIOR-ART-DISCLOSED:

U.S. PATENT DOCUMENTS

Search Selected Search ALL Clear

	PAT-NO	ISSUE-DATE	PATENTEE-NAME	US-CL
☐	3764992	October 1973	Milne	364/DIG.1
☐	4851987	July 1989	Day	395/550
☐	5021950	June 1991	Nishikawa	364/200
☐	5167024	November 1992	Smith et al.	395/375
☐	5203003	April 1993	Donner	395/800

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☐	5218704	June 1993	Watts, Jr. et al.	395/750
☐	5247655	September 1993	Khan et al.	395/550
☐	5291542	March 1994	Kivari et al.	379/58
☐	5390350	February 1995	Chung et al.	395/150

FOREIGN PATENT DOCUMENTS

FOREIGN-PAT-NO	PUBN-DATE	COUNTRY	US-CL
0 451 661 A2	October 1991	EP	
WO 92/09028	May 1992	WO	

OTHER PUBLICATIONS

Intel 486 DX2 Microprocessor Data Book, pp. 1-4, 1-6, 1-7, 2-1, 6-1, 6-2, 6-5, and 14-3.
Intel Microprocessors, vol. 1, 1992, various pages, section 6.

ART-UNIT: 277

PRIMARY-EXAMINER: Butler; Dennis M.

ATTY-AGENT-FIRM: Neerings; Ronald O. Kesterson; James C. Donaldson; Richard L.

ABSTRACT:

A method and apparatus (10) for changing processor clock rate are provided in which control signals operate to change the rate of a clock signal output by clock switching logic (26). A processor (24) floats a system bus after the clock signal is changed. After the processor (24) has locked onto the new clock rate it is permitted to resume activity on the system bus.

50 Claims, 21 Drawing figures

L4: Entry 22 of 47 File: USPT Jul 21, 1998

DOCUMENT-IDENTIFIER: US 5784598 A
**** See image for Certificate of Correction ****
TITLE: Method and apparatus for changing processor clock rate

Detailed Description Text (23):
As described above, the clock switching logic 26 may also be used to change the processor clock rate to a rate other than zero. This is performed by causing the processor to float the bus through the use of the backoff signal and changing the clock speed, which will result in the generation of the OUT+ signal to clear BOFF+ and then release of the backoff pin, causing the processor to resume control of the bus after the processor has locked onto the new clock rate. The maximum clock rate may be restored by increasing the clock rate, causing the processor to float the bus, allowing the processor to lock onto the new rate, and then having the processor resume activity on the bus, as described above.

CLAIMS:

4. The method of claim 3, and further comprising the step of monitoring the processor's activity to generate the request to restore the pre-change clock rate.

5. The method of claim 2, and further comprising the step of monitoring the processor's activity to generate the request to change the clock rate.

7. The method of claim 1, and further comprising the step of monitoring the processor's activity to generate the request to change the processor clock rate.

10. The method of claim 9, and further comprising the step of monitoring the processor's activity to generate the request to restore the pre-change clock rate.

13. The method of claim 12, and further comprising the step of monitoring the processor's activity to generate the request to restore the pre-change clock rate.

16. The method of claim 15, and further comprising the step of monitoring the processor's activity to generate the request to restore the pre-change processor clock rate.

17. The method of claim 14, and further comprising the step of monitoring the processor's activity to generate the request to change the clock rate.

19. The method of claim 11, and further comprising the step of monitoring the processor's activity to generate the request to change the processor clock rate.

23. The circuit of claim 21, and further comprising circuitry for monitoring the processor's activity and operable to generate said request to change said processor clock rate.

26. The circuit of claim 25, and further comprising circuitry for monitoring the processor's activity and operable to generate said request to restore said pre-change processor clock rate.

29. The circuit of claim 26, and further comprising circuitry for monitoring the processor's activity and operable to generate said request to restore said pre-change processor clock rate.

30. The circuit of claim 27, and further comprising circuitry for monitoring said processor's activity and operable to generate said request to change said clock rate.

39. The circuit of claim 38, and further comprising circuitry for monitoring the processor's activity and operable to generate said request to restore said pre-change processor clock rate.

41. The circuit of claim 37, and further comprising circuitry for monitoring the processor's activity and operable to generate said request to change said processor clock rate.

44. The circuit of claim 43, and further comprising circuitry for monitoring the processor's activity and operable to generate said request to restore said pre-change processor clock rate.

45. The circuit of claim 42, and further comprising circuitry for monitoring said processor's activity and operable to generate said request to change said clock rate.

First Hit Fwd Refs

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L4: Entry 21 of 47 File: USPT Sep 15, 1998

DOCUMENT-IDENTIFIER: US 5809293 A
TITLE: System and method for program execution tracing within an integrated processor

Brief Summary Text (4):
The increase in use of very large scale integrated ("VLSI") circuit technologies has enabled the integration of entire systems and sub-systems onto a single chip. This integration has led to increased performance on critical processor data and instruction buses through the use of internal data and instruction caches. However, a negative result of this increased integration is a significantly reduced ability to easily access particular buses needed for monitoring processor activity. For instance, an instruction cached design inhibits the ability to monitor and capture the program instruction flow since the instructions are fetched from an embedded cache instead of memory external to the processor. In fact, for efficient cache designs, there is a high probability that the instructions will reside in cache and will not be visible from the external pins of the microprocessor. It is also possible that the entire program may reside in embedded cache, thereby making it virtually impossible to follow instruction execution externally.

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Search Results - Record(s) 1 through 10 of 26 returned.

☐ 1. Document ID: US 6230279 B1

L7: Entry 1 of 26 File: USPT May 8, 2001

US-PAT-NO: 6230279
DOCUMENT-IDENTIFIER: US 6230279 B1

TITLE: System and method for dynamically controlling processing speed of a computer in response to user commands

DATE-ISSUED: May 8, 2001

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Dewa; Koichi	Tokyo			JP
Yamaki; Masayo	Tokyo			JP
Sato; Fumitaka	Tokyo			JP

ASSIGNEE-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY	TYPE CODE
Kabushiki Kaisha Toshiba	Kawasaki			JP	03

APPL-NO: 09/ 563820 [PALM]
DATE FILED: May 3, 2000

PARENT-CASE:
This is a continuation of application Ser. No. 09/073,808, filed May 7, 1998 now U.S. Pat. No. 6,081,901 incorporate herein by reference.

FOREIGN-APPL-PRIORITY-DATA:

COUNTRY	APPL-NO	APPL-DATE
JP	9-145253	June 3, 1997

INT-CL: [07] G06 F 1/32

US-CL-ISSUED: 713/324; 713/322
US-CL-CURRENT: 713/324; 713/322

FIELD-OF-SEARCH: 712/240, 713/300, 713/320, 713/322, 713/323, 713/324, 713/321

PRIOR-ART-DISCLOSED:

U.S. PATENT DOCUMENTS

h e b b cg b e e ch

PAT-NO	ISSUE-DATE	PATENTEE-NAME	US-CL
4137563	January 1979	Tsunoda	
4381552	April 1983	Nocilini et al.	
4851897	July 1989	Inuma et al.	358/29
5142684	August 1992	Perry et al.	
5222239	June 1993	Rosch	
5228131	July 1993	Veda et al.	712/240
5452401	September 1995	Lin	
5504910	April 1996	Wisor et al.	
5560017	September 1996	Barrett et al.	
5586332	December 1996	Jain et al.	713/322
5664201	September 1997	Ikedea	
5719800	February 1998	Mittal et al.	713/321
5737613	April 1998	Mensch, Jr.	
5740417	April 1998	Kennedy et al.	712/240
5742832	April 1998	Buxton et al.	
5761517	June 1998	Durham et al.	
5768602	June 1998	Dhuey	
5812860	September 1998	Horden et al.	
5826092	October 1998	Flannery	
5887178	March 1999	Tsujimoto et al.	
5951689	September 1999	Evoy et al.	713/322
6081901	June 2000	Dewa et al.	713/300
6108776	August 2000	Check et al.	712/240

ART-UNIT: 271

PRIMARY-EXAMINER: Auve; Glenn A.

ATTY-AGENT-FIRM: Finnegan, Henderson, Farabow, Garrett & Dunner, L.L.P.

ABSTRACT:

When a user instructs acceleration or deceleration of the CPU processing speed with an "accelerator" button or a "brake" button, a speed control MMI informs power management system software of the corresponding information to change the CPU processing speed. The change is recorded on a speed management database in correspondence with the name of the application program which is currently being executed. Every time acceleration or deceleration of the CPU processing speed is instructed by the user, speed management data is formed on the speed management database. By using the speed management data, the CPU processing speed can be dynamically controlled for each piece of software when it is executed. Further disclosed is a novel power dissipation control system for a microprocessor, adapted to be used in conjunction with the above described MMI.

19 Claims, 14 Drawing figures

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☐ 2. Document ID: US 6076158 A

L7: Entry 2 of 26 File: USPT Jun 13, 2000

US-PAT-NO: 6076158
DOCUMENT-IDENTIFIER: US 6076158 A

TITLE: Branch prediction in high-performance processor

DATE-ISSUED: June 13, 2000

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Sites; Richard Lee	Boylston	MA		
Witek; Richard T.	Littleton	MA		

ASSIGNEE-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY	TYPE CODE
Digital Equipment Corporation	Houston	TX			02

APPL-NO: 08/ 086354 [PALM]
DATE FILED: July 1, 1993

PARENT-CASE:
This application is a continuation of Ser. No. 07/547,589 filed Jun. 29, 1990, abandoned.

INT-CL: [07] G06 F 9/32

US-CL-ISSUED: 712/230
US-CL-CURRENT: 712/230

FIELD-OF-SEARCH: 395/375

PRIOR-ART-DISCLOSED:

U.S. PATENT DOCUMENTS

PAT-NO	ISSUE-DATE	PATENTEE-NAME	US-CL
4402042	August 1983	Guttag	395/375
4755966	July 1988	Lee et al.	395/375
4777594	October 1988	Jones et al.	395/375
4876642	October 1989	Gibson	395/375
4945511	July 1990	Itomitsu	395/375
5129068	July 1992	Watanabe et al.	395/400
5142634	August 1992	Fite et al.	395/375
5155820	October 1992	Gibson	395/375
5193156	March 1993	Yoshida et al.	395/375

FOREIGN PATENT DOCUMENTS

FOREIGN-PAT-NO	PUBN-DATE	COUNTRY	US-CL
207 665	January 1987	EP	
320 098	June 1989	EP	
61-208 129	February 1987	JP	

OTHER PUBLICATIONS

Intek product specification, "i860.TM. 64-Bit Microprocessor", Oct. 1989, pp. 5-1 to 5-72.
Kane, "MIPS R2000 RISC Architecture", Prentice Hall, 1987, pp. 1-1 to 4-11 and pp. A-1 to A-9.
Radin, "The 801 Minicomputer", IBM Research Report, Nov. 11, 1981, pp. 1-23 .

ART-UNIT: 273

PRIMARY-EXAMINER: Teska; Kevin J.

ASSISTANT-EXAMINER: Choi; Kyle J.

ATTY-AGENT-FIRM: Hamilton, Brook, Smith & Reynolds, P.C.

ABSTRACT:

A CPU of the RISC type employs a standardized, fixed instruction size, and permits only simplified memory access data width and addressing modes limited to register-to-register operations and register load/store operations. Byte manipulation instructions include the facility for doing in-register byte extract, insert and masking, along with non-aligned load and store instructions. The load/locked and store/conditional instructions permits the implementation of atomic byte writes. By providing a conditional move instruction, many short branches can be eliminated altogether. A conditional move instruction tests a register and moves a second register to a third if the condition is met; this function can be substituted for short branches and thus maintain the sequentiality of the instruction stream. Performance can be speeded up by predicting the target of a branch and prefetching the new instruction based upon this prediction; a branch prediction rule is followed that requires all forward branches to be predicted not-taken and all backward branches to be predicted as taken. Another embodiment uses unused bits in the standard-sized instruction to provide a hint of the expected target address for jump and jump to subroutine instructions or the like. The target can thus be prefetched before the actual address has been calculated and placed in a register. In addition, the unused displacement part of the jump instruction can contain a field to define the actual type of jump, i.e., jump, jump to subroutine, return from subroutine, and thus place a predicted target address in a stack to allow prefetching before the instruction has been executed. The processor can employ a variable memory page size, so that the entries in a translation buffer for implementing virtual addressing can be optimally used. A granularity hint is added to the page table entry to define the page size for this entry. An additional feature is the addition of a prefetch instruction which serves to move a block of data to a faster-access cache in the memory hierarchy before the data block is to be used.

10 Claims, 11 Drawing figures

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☐ 3. Document ID: US 5991883 A

L7: Entry 3 of 26 File: USPT Nov 23, 1999

US-PAT-NO: 5991883
DOCUMENT-IDENTIFIER: US 5991883 A

TITLE: Power conservation method for a portable computer with LCD display

DATE-ISSUED: November 23, 1999

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Atkinson; Lee	Houston	TX		

ASSIGNEE-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY	TYPE CODE
Compaq Computer Corporation	Houston	TX			02

APPL-NO: 08/ 685093 [PALM]
DATE FILED: July 23, 1996

PARENT-CASE:
This application claims priority from provisional application Ser. No. 60/019,108 filed Jun. 3, 1996 and provisional application Ser. No. 60/019,613 filed Jun. 11, 1996.

INT-CL: [06] G06 F 1/00

US-CL-ISSUED: 713/300; 713/320, 713/322, 713/340, 345/509, 707/526
US-CL-CURRENT: 713/300; 345/501, 713/320, 713/322, 713/340, 715/526

FIELD-OF-SEARCH: 395/750.01, 395/375, 395/800, 395/750.04, 395/750.08, 371/66, 707/526, 345/509

PRIOR-ART-DISCLOSED:

U.S. PATENT DOCUMENTS

PAT-NO	ISSUE-DATE	PATENTEE-NAME	US-CL
5136695	August 1992	Goldshlang et al.	345/509
5167024	November 1992	Smith et al.	395/375
5218607	June 1993	Saito et al.	371/66
5369771	November 1994	Gettel	
5392438	February 1995	Gunji	395/750
5442800	August 1995	Okamura	395/800
5465367	November 1995	Reddy et al.	395/750
5524249	June 1996	Suboh	395/750
5537650	July 1996	West et al.	395/750
5560024	September 1996	Harper et al.	395/750
5572655	November 1996	Tuljapurkar et al.	395/788

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5615376	March 1997	Ranganathan	395/750
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5625826	April 1997	Atkinson	395/750

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Advanced Power Management (APM) BIOS Interface Specification, Revision 1.2, Feb. 1996, Intel Corporation, Microsoft Corporation.
Power Management Coordinator API Specification, Revision 1.00, Apr. 8, 1994, Intel Corporation.
Volkman, Victor R. "Advanced Power Management for DOS" Developer's Preview, Jul. 1992, pp. 19-23.
Caruthers, Frank, editor, "Battery-Management Circuitry Gets Smarter" Computer Design's OEM Integration, May 1994, pp. 15-18.

ART-UNIT: 271

PRIMARY-EXAMINER: Sheikh; Ayaz R.

ASSISTANT-EXAMINER: Thlang; Eric S.

ATTY-AGENT-FIRM: Groover; Robert

ABSTRACT:

A system and process for power conservation in a portable computer system. When the application or hardware in use allows for reduced video performance, the refresh rate of the video graphics controller is reduced to a level which allows practical use of the display but consumes much less power than a normal mode.

47 Claims, 3 Drawing figures

☐ 4. Document ID: US 5784598 A

L7: Entry 4 of 26 File: USPT Jul 21, 1998

US-PAT-NO: 5784598
DOCUMENT-IDENTIFIER: US 5784598 A
**** See image for Certificate of Correction ****

TITLE: Method and apparatus for changing processor clock rate

DATE-ISSUED: July 21, 1998

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Griffith; Jenni L.	Belton	TX		

ASSIGNEE-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY	TYPE CODE
Texas Instruments Incorporated	Dallas	TX			02

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APPL-NO: 08/ 479580 [PALM]
DATE FILED: June 7, 1995

PARENT-CASE:
This application is a Continuation of application Ser. No. 07/897,693 filed Jun. 12, 1992, now abandoned.

INT-CL: [06] G06 F 1/08

US-CL-ISSUED: 395/556; 395/560
US-CL-CURRENT: 713/501; 713/601

FIELD-OF-SEARCH: 395/550, 395/750, 395/555, 395/556, 395/559, 395/560, 395/750.04

PRIOR-ART-DISCLOSED:

U.S. PATENT DOCUMENTS

PAT-NO	ISSUE-DATE	PATENTEE-NAME	US-CL
3764992	October 1973	Milne	364/DIG.1
4851987	July 1989	Day	395/550
5021950	June 1991	Nishikawa	364/200
5167024	November 1992	Smith et al.	395/375
5203003	April 1993	Donner	395/800
5218704	June 1993	Watts, Jr. et al.	395/750
5247655	September 1993	Khan et al.	395/550
5291542	March 1994	Kivari et al.	379/58
5390350	February 1995	Chung et al.	395/150

FOREIGN PATENT DOCUMENTS

FOREIGN-PAT-NO	PUBN-DATE	COUNTRY	US-CL
0 451 661 A2	October 1991	EP	
WO 92/09028	May 1992	WO	

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Intel 486 DX2 Microprocessor Data Book, pp. 1-4, 1-6, 1-7, 2-1, 6-1, 6-2, 6-5, and 14-3.
Intel Microprocessors, vol. 1, 1992, various pages, section 6.

ART-UNIT: 277

PRIMARY-EXAMINER: Butler; Dennis M.

ATTY-AGENT-FIRM: Neerings; Ronald O. Kesterson; James C. Donaldson; Richard L.

ABSTRACT:

A method and apparatus (10) for changing processor clock rate are provided in which

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control signals operate to change the rate of a clock signal output by clock switching logic (26). A processor (24) floats a system bus after the clock signal is changed. After the processor (24) has locked onto the new clock rate it is permitted to resume activity on the system bus.

50 Claims, 21 Drawing figures

Full | Title | Citation | Front | Review | Classification | Date | Reference | Claims | KWMC | Draw De

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☐ 5. Document ID: US 5740417 A

L7: Entry 5 of 26 File: USPT Apr 14, 1998

US-PAT-NO: 5740417
DOCUMENT-IDENTIFIER: US 5740417 A

TITLE: Pipelined processor operating in different power mode based on branch prediction state of branch history bit encoded as taken weakly not taken and strongly not taken states

DATE-ISSUED: April 14, 1998

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Kennedy; A. Richard	Austin	TX		
Croxton; Cody B.	Georgetown	TX		

ASSIGNEE-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY	TYPE CODE
Motorola, Inc.	Schaumburg	IL			02

APPL-NO: 08/ 567591 [PALM]
DATE FILED: December 5, 1995

INT-CL: [06] G06 F 9/38

US-CL-ISSUED: 395/586; 395/587
US-CL-CURRENT: 712/239; 712/240

FIELD-OF-SEARCH: 395/586, 395/587

PRIOR-ART-DISCLOSED:

U.S. PATENT DOCUMENTS

PAT-NO	ISSUE-DATE	PATENTEE-NAME	US-CL
5163140	November 1992	Stiles et al.	
5175827	December 1992	Morisada	
5210831	May 1993	Emma et al.	
5228131	July 1993	Ueda et al.	
5230068	July 1993	Van Dyke et al.	

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5317702	May 1994	Morisada	
5392437	February 1995	Matter et al.	
5394529	February 1995	Brown, III et al.	395/587
5423011	June 1995	Blaner et al.	395/587
5577217	November 1996	Hoyt et al.	395/376
5584001	December 1996	Hoyt et al.	395/585
5606676	February 1997	Grochowski et al.	395/586

ART-UNIT: 235

PRIMARY-EXAMINER: Lim; Krisna

ATTY-AGENT-FIRM: Polansky; Paul J.

ABSTRACT:

A low-power pipelined data processor (20) includes a branch prediction mechanism for speculatively placing branch target instructions into the fetch, decode, dispatch, and execute pipeline when a branch is predicted to be taken. To save power the data processor (20) selectively disables one or more pipeline resources (24) associated with placing the branch target instructions into the pipeline according to the strength of the prediction. If the prediction is weakly not taken, the data processor (20) enables the pipeline resource (24) to prevent disruptions to the pipeline if the branch resolves as taken during the cycle. However if the prediction is strongly not taken, the pipeline resource (24) is disabled to save power, which outweighs the infrequent resolution to taken. In one embodiment, the data processor (20) disables a branch target instruction cache (24) if history bits corresponding to the branch instruction stored in a branch history table (26) indicate strongly that the branch will not be taken.

14 Claims, 2 Drawing figures

☐ 6. Document ID: US 5655127 A

L7: Entry 6 of 26 File: USPT Aug 5, 1997

US-PAT-NO: 5655127
DOCUMENT-IDENTIFIER: US 5655127 A

TITLE: Method and apparatus for control of power consumption in a computer system

DATE-ISSUED: August 5, 1997

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Rabe; Jeffrey L.	Rancho Cordova	CA		
Bogin; Zohar	Folsom	CA		
Bhatt; Ajay V.	El Dorado Hills	CA		
Kardach; James P.	San Jose	CA		

Shah; Nilesh V. Folsom CA

ASSIGNEE-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY	TYPE CODE
Intel Corporation	Santa Clara	CA			02

APPL-NO: 08/ 612673 [PALM]
DATE FILED: March 8, 1996

PARENT-CASE:
This is a continuation of application Ser. No. 08/191,651, filed Feb. 4, 1994, now abandoned.

INT-CL: [06] G06 F 1/26

US-CL-ISSUED: 395/750.04; 345/838, 345/868, 345/734
US-CL-CURRENT: 713/322; 710/18, 710/261, 710/48

FIELD-OF-SEARCH: 395/750, 395/838, 395/868, 395/734

PRIOR-ART-DISCLOSED:

U.S. PATENT DOCUMENTS

PAT-NO	ISSUE-DATE	PATENTEE-NAME	US-CL
3623017	November 1971	Lowell et al.	
3715729	February 1973	Mercy	
3736569	May 1973	Bouricius et al.	395/750
3737637	June 1973	Frankeny et al.	371/28
3895311	July 1975	Basse et al.	
3919695	November 1975	Gooding	
3931585	January 1976	Barker et al.	
3936762	February 1976	Cox, Jr. et al.	
4077016	February 1978	Sanders et al.	
4095267	June 1978	Morimoto	
4203153	May 1980	Boyd	
4264863	April 1981	Kojima	
4293927	October 1981	Hoshii	
4300019	November 1981	Toyomaki	
4365290	December 1982	Nelms et al.	
4405898	September 1983	Flemming	
4479191	October 1984	Nojima et al.	
4545030	October 1985	Kitchin	
4615005	September 1986	Maejima et al.	
4638452	January 1987	Schultz et al.	
4639864	January 1987	Katzman et al.	
4667289	May 1987	Yoshida et al.	
4669099	May 1987	Zinn	
4698748	October 1987	Juzswik et al.	

4758945	July 1988	Remedi	
4763294	August 1988	Fong	
4766597	August 1988	Kato	
4780843	October 1988	Tietjen	
4814591	March 1989	Nara et al.	
4823292	April 1989	Hillion	
4841440	June 1989	Yonezu et al.	
4881205	November 1989	Aihara	
4896260	January 1990	Hyatt	
4907183	March 1990	Tanaka	
4922450	May 1990	Rose et al.	
4935863	June 1990	Calvas et al.	
4979097	December 1990	Triolo et al.	
4980836	December 1990	Carter et al.	364/483
4983966	January 1991	Grone et al.	
4991129	February 1991	Swartz	
5021679	June 1991	Fairbanks et al.	
5059924	October 1991	Check	
5077686	December 1991	Rubinstein	
5083266	January 1992	Watanabe	395/275
5103114	April 1992	Fitch	
5123107	June 1992	Mensch, Jr.	
5129091	July 1992	Yorimoto et al.	
5133064	July 1992	Hotta et al.	
5151992	September 1992	Nagae	
5167024	November 1992	Smith et al.	395/375
5175845	December 1992	Little	
5189647	February 1993	Suzuki et al.	
5220672	June 1993	Nakao et al.	
5239652	August 1993	Seibert et al.	
5249298	September 1993	Bolan et al.	
5251320	October 1993	Kuzawinski et al.	
5263028	November 1993	Borgnis et al.	
5319771	June 1994	Takeda	
5329621	July 1994	Burgess et al.	
5335168	August 1994	Walker	364/707
5336939	August 1994	Eitrheim et al.	
5355501	October 1994	Gross et al.	
5359232	October 1994	Eitrheim et al.	
5369771	November 1994	Gettel	395/750
5396635	March 1995	Fung	395/800
5404546	April 1995	Stewart	
5428754	June 1995	Baldwin	
5461652	October 1995	Hongo	

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FOREIGN-PAT-NO	PUBN-DATE	COUNTRY	US-CL
0103755	August 1983	EP	
0140814	May 1984	EP	
0242010	December 1987	EP	
0368144	February 1989	EP	
0366250	September 1989	EP	
0419908	June 1990	EP	
0451661	March 1991	EP	
0478132	December 1991	EP	
0654726	October 1994	EP	
9302408	February 1993	DE	
2010551	November 1978	GB	
2130765	October 1983	GB	

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Case, Brian, "R4000 Extends R3000 Architecture With 64-bit Capabilities", Microprocessor Report, vol.: v5, Issue: n19, p10(4), Oct. 16, 1991.
Wilson, Ron, "MIPS Rethinks RISC With Superpipelining", Computer Design, vol.: v30, Issue: n3, p28(3), Feb. 1, 1991.
Intel Automotive Components Handbook, "Power-On Reset", 1988, pp. 10-24 & 10-25.
Motorola MC6802032--Bit Microprocessor User's Manual, 3rd Edition, 1990, pp. 1-3.

ART-UNIT: 235

PRIMARY-EXAMINER: Auve; Glenn A.

ASSISTANT-EXAMINER: Seto; Jeffrey K.

ATTY-AGENT-FIRM: Blakely, Sokoloff, Taylor & Zafman

ABSTRACT:

A computer system having a responsive low-power mode and a full-power mode of operation. The computer system includes a power consumption controller, a processor and a communication device. The power consumption controller generates an interrupt signal in response to a low power event or a fully operational event. The power consumption controller also generates a clock control signal. The clock control signal is deasserted during the full-power mode of operation and alternatively asserted for a first duration and deasserted for a second duration during the low-power mode of operation. In response to an asserted clock control signal, the processor suppresses the internal clock signal to at least one functional block within the processor and in response to a deasserted clock control signal, the processor transmits the internal clock signal to at least one functional block within the processor. By transmitting the internal clock signal to at least one functional block within the processor during the low-power mode of operation, the processor may respond to communication signals from a communication device during the low-power mode of operation.

18 Claims, 10 Drawing figures

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☐ 7. Document ID: US 5544082 A

L7: Entry 7 of 26 File: USPT Aug 6, 1996

US-PAT-NO: 5544082
DOCUMENT-IDENTIFIER: US 5544082 A

TITLE: Method and system for placing a computer in a reduced power state

DATE-ISSUED: August 6, 1996

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Garcia-Duarte; Fernando	Redmond	WA		
Hensley; John	Redmond	WA		
Mohanraj; Shanmugam	Redmond	WA		
Subramaniyan; Nagarajan	Redmond	WA		
Olsson; David B.	Seattle	WA		

ASSIGNEE-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY	TYPE CODE
Microsoft Corporation	Redmond	WA			02

APPL-NO: 08/ 388952 [PALM]
DATE FILED: February 15, 1995

PARENT-CASE:
CROSS-REFERENCE TO RELATED APPLICATION This application is a continuation of U.S. Patent application Ser. No. 07/958/050, filed Oct. 6, 1992 now U.S. Pat. No. 5,416,726.

INT-CL: [06] G06 F 1/32

US-CL-ISSUED: 364/707; 364/273.2, 364/483, 395/750, 395/775, 395/183.14
US-CL-CURRENT: 713/321; 702/186, 713/323, 714/38

FIELD-OF-SEARCH: 395/750, 395/775, 371/19, 371/16.1, 371/29.1, 371/23, 371/18, 364/483, 364/550, 364/707, 364/273.2, 364/948.4, 364/948.91

PRIOR-ART-DISCLOSED:

U.S. PATENT DOCUMENTS

PAT-NO	ISSUE-DATE	PATENTEE-NAME	US-CL
4698748	October 1987	Juzswik et al.	364/200
4974180	November 1990	Patton et al.	364/550
4980836	December 1990	Carter et al.	364/483
5083266	January 1992	Watanabe	395/275
5119377	June 1992	Cobb et al.	371/19

5218704	June 1993	Watts, Jr. et al.	395/750
5239652	August 1993	Seibert et al.	395/750
5416726	May 1995	Garcia-Duarte et al.	364/550

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Glass, Brett, "Under The Hood", BYTE, Sep., 1991, pp. 329-335.
Volkman, Victor R., "Advanced Power Management for DOS", Developer's Journal, Jul., 1992, pp. 19-23.

ART-UNIT: 244

PRIMARY-EXAMINER: Voeltz; Emanuel T.

ASSISTANT-EXAMINER: Miller; Craig Steven

ATTY-AGENT-FIRM: Seed and Berry LLP

ABSTRACT:

A method and system for placing a computer in a reduced power state is provided. In a preferred embodiment of the present invention, the system monitors the performance of a monitored activity of a program executing. The system determines whether the program is performing the monitored activity regularly. If the program is performing the monitored activity regularly, the system places the computer in a reduced power state.

53 Claims, 16 Drawing figures

☐ 8. Document ID: US 5504908 A

L7: Entry 8 of 26 File: USPT Apr 2, 1996

US-PAT-NO: 5504908
DOCUMENT-IDENTIFIER: US 5504908 A

TITLE: Power saving control system for computer system

DATE-ISSUED: April 2, 1996

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Ikeda; Osamu	Tokyo			JP

ASSIGNEE-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY	TYPE CODE
Dia Semicon Systems Incorporated	Tokyo			JP	03

APPL-NO: 08/ 039869 [PALM]
DATE FILED: March 30, 1993

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FOREIGN-APPL-PRIORITY-DATA:

COUNTRY	APPL-NO	APPL-DATE
JP	4-080807	April 2, 1992

INT-CL: [06] G06 F 1/32

US-CL-ISSUED: 395/750; 365/227, 364/707
US-CL-CURRENT: 713/300; 365/227, 713/321

FIELD-OF-SEARCH: 395/750, 395/550, 395/575, 364/707, 365/226, 365/227

PRIOR-ART-DISCLOSED:

U.S. PATENT DOCUMENTS

PAT-NO	ISSUE-DATE	PATENTEE-NAME	US-CL
4718043	January 1988	Akatsuka	365/227
4980836	December 1990	Carter et al.	364/483
5142684	August 1992	Perry et al.	395/750
5148546	September 1992	Blodgett	395/750
5168151	December 1992	Nara	235/492
5222239	June 1993	Rosch	395/750
5369771	November 1994	Gettel	395/750
5388265	February 1995	Volk	395/750
5390334	February 1995	Harrison	395/750
5394558	February 1995	Arakawa et al.	395/800
5404543	April 1995	Faucher et al.	395/750
5426755	June 1995	Yokouchi et al.	395/425
5430881	July 1995	Ikeda	395/750

ART-UNIT: 235

PRIMARY-EXAMINER: Auve; Glenn A.

ATTY-AGENT-FIRM: Barnes & Thornburg

ABSTRACT:

A power saving control system for a computer system including a CPU, is provided with a mode selecting circuit for selectively operating the CPU in a first mode with relatively high performance and high power consumption and a second mode with relatively low performance and low power consumption, a repeated access detecting circuit for monitoring addresses accessed by the CPU over a given period in order to detect a predetermined operational state of the CPU, in which only specific address group is repeatedly accessed, a control circuit associated with the first means for normally operating the first means in the first mode and responsive to the second means detecting the predetermined operational state, for operating the first means in the second mode as long as the predetermined operational state is maintained, and a state display for generating an indication perceptible by an operator of the computer system indicating current operational mode of the CPU.

15 Claims, 2 Drawing figures

Full | Title | Citation | Front | Review | Classification | Date | Reference | Claims | KWMC | Draw De

☐ 9. Document ID: US 5487181 A

L7: Entry 9 of 26 File: USPT Jan 23, 1996

US-PAT-NO: 5487181
DOCUMENT-IDENTIFIER: US 5487181 A

TITLE: Low power architecture for portable and mobile two-way radios

DATE-ISSUED: January 23, 1996

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Dailey; Timothy E.	Forest	VA		
Dissosway; Marc A.	Forest	VA		
Croucher; Russell L.	Forest	VA		

ASSIGNEE-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY	TYPE CODE
Ericsson GE Mobile Communications Inc.	Lynchburg	VA			02

APPL-NO: 07/ 969739 [PALM]
DATE FILED: October 28, 1992

INT-CL: [06] H04 B 1/40, H04 B 7/32

US-CL-ISSUED: 455/89; 455/90, 455/343, 364/228.6, 364/230.2, 364/DIG.1
US-CL-CURRENT: 455/90.2; 455/557, 455/574, 712/32

FIELD-OF-SEARCH: 455/38.3, 455/343, 455/89-90, 455/73, 455/76, 455/183.2, 455/127, 379/58, 345/89, 345/148, 370/110.2, 364/228.4-228.6, 364/230.2

PRIOR-ART-DISCLOSED:

U.S. PATENT DOCUMENTS

PAT-NO	ISSUE-DATE	PATENTEE-NAME	US-CL
4384361	May 1983	Masaki	455/31
4437095	March 1984	Akahori et al.	340/825.44
4562307	December 1985	Bursztejn et al.	379/61
4598258	July 1986	Babano	331/14
4731814	March 1988	Becker et al.	379/62
4830832	April 1989	Nagata et al.	455/343
4870699	December 1989	Garner	455/76
4887311	December 1989	Garner et al.	455/76
4901036	February 1990	Herold et al.	455/183.2

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4903319	February 1990	Kasai et al.	455/33
4947454	August 1990	Garner	455/88
4977611	December 1990	Maru	455/161
4979102	December 1990	Tokuume	364/200
5001776	March 1991	Clark	455/343
5058203	October 1991	Inagami	455/89
5109537	April 1992	Toki	455/343
5159765	October 1992	Critchlow	455/76
5170490	December 1992	Cannon et al.	455/343
5175759	December 1992	Metroka	379/58
5241537	August 1993	Gulliford et al.	370/110.2
5280650	January 1994	Sobti	455/38.3
5295178	March 1994	Nickel et al.	379/58
5327580	July 1994	Vignali et al.	455/15

FOREIGN PATENT DOCUMENTS

FOREIGN-PAT-NO	PUBN-DATE	COUNTRY	US-CL
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OTHER PUBLICATIONS

"M-PD System . . . 136-174 MHz Personal Two-Way FM Radio Combination"; Maintenance Manual; GE Mobile Communications; LBI-31629A, May 1987.
Hitachi H8/532 HD6475328, HD6435328 Hardware Manual (Jan. 1992).
Hitachi Single-Chip Microcomputer H8/330 HD6473308, HD6433308 Hardware Manual--User's Manual (Dec. 1989).

ART-UNIT: 261

PRIMARY-EXAMINER: Pham; Chi H.

ATTY-AGENT-FIRM: Nixon & Vanderhye

ABSTRACT:

An extremely compact, full featured portable radio architecture conserves power by allowing a processor to sleep except when it needs to perform tasks. A lower power processor which acts principally as an interrupt controller but which performs other functions as well (e.g., tone decode, synthesizer lock monitoring, etc.) so the main processor can sleep as much as possible and yet is assured of being awoken promptly when its processing power is required. The resulting portable radio has extremely low power consumption (e.g., on the order of 75 milliamperes during trunked mode operation)--thereby permitting even a relatively small battery pack to provide nearly 8 hours of continuous operation. The portable radio with battery is small and lightweight enough to fit into a front shirt pocket.

35 Claims, 19 Drawing figures

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☐ 10. Document ID: US 5239652 A

L7: Entry 10 of 26 File: USPT Aug 24, 1993

US-PAT-NO: 5239652
DOCUMENT-IDENTIFIER: US 5239652 A

TITLE: Arrangement for reducing computer power consumption by turning off the microprocessor when inactive

DATE-ISSUED: August 24, 1993

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Seibert; Mark H.	Cupertino	CA		
Wallgren; Markus C.	Palo Alto	CA		

ASSIGNEE-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY	TYPE CODE
Apple Computer, Inc.	Cupertino	CA			02

APPL-NO: 07/ 650053 [PALM]
DATE FILED: February 4, 1991

INT-CL: [05] G06F 15/00, G06F 11/30

US-CL-ISSUED: 395/750; 364/707, 364/DIG.1, 364/273.1, 364/241
US-CL-CURRENT: 713/323; 360/69, 713/321

FIELD-OF-SEARCH: 395/750, 364/707, 364/141, 364/191, 364/701

PRIOR-ART-DISCLOSED:

U.S. PATENT DOCUMENTS

PAT-NO	ISSUE-DATE	PATENTEE-NAME	US-CL
4698748	October 1987	Juzswik et al.	364/200
4769768	September 1988	Bomba et al.	395/725
4809163	February 1989	Hirosawa et al.	395/750
4851987	July 1989	Day	395/550
4870570	September 1989	Satoh et al.	395/750
4965738	October 1990	Bauer et al.	364/483
5142684	August 1992	Perry et al.	395/750

ART-UNIT: 232

PRIMARY-EXAMINER: Harrell; Robert B.

ASSISTANT-EXAMINER: Geckil; Mehmet

ATTY-AGENT-FIRM: Blakely, Sokoloff, Taylor & Zafman

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ABSTRACT:

A power consumption reduction method and apparatus for a computer is described. The operating system running on the CPU of the computer determines when the CPU is not actively processing and generates a power-off signal to a control logic circuit. The control logic circuit then disconnects the CPU from the power supply. Pulses sent by a periodic timer or interrupts from input/output units are applied to the control logic circuit to at least periodically issue a power-on signal to the CPU. Power is supplied to the CPU for a given time period at every power-on signal. During this period, the CPU executes miscellaneous housekeeping chores including the polling of disk drives and determines when the CPU should resume normal processing. The control logic circuit also determines, at every power-on signal, whether the CPU is already on or being turned off. The control logic circuit will not issue a reset signal to enable the reset of the CPU if it is already on. If, however, the CPU has been turned off by the operating system, the control logic circuit will reset the CPU at every periodic power-on signal until CPU resumes its normal operation.

8 Claims, 11 Drawing figures

Terms	Documents
(4085449| 4317181| 4417320| 4531826| 4670837| 4698748| 4819164| 4980836| 5072376| 5125088| 5142684| 5153535| 5163143| 5167024| 5218704| 5239641| 5239652| 5487181| 5504908| 5544082| 5655127| 5740417| 5784598| 5991883| 6076158| 6230279)![pn]	26

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US005809293A

United States Patent [19]

Bridges et al.

[11] **Patent Number: 5,809,293**

[45] **Date of Patent: Sep. 15, 1998**

[54] **SYSTEM AND METHOD FOR PROGRAM EXECUTION TRACING WITHIN AN INTEGRATED PROCESSOR**

[75] Inventors: **Jeffrey Todd Bridges**, Raleigh; **Thomas K. Collopy**, Cary; **James N. Dieffenderfer**, Apex; **Thomas Joseph Irens**, Raleigh; **Harry L. Linzer**, Raleigh; **Thomas Andrew Sartorius**, Raleigh, all of N.C.

[73] Assignee: **International Business Machines Corporation**, Armonk, N.Y.

[21] Appl. No.: **283,128**

[22] Filed: **Jul. 29, 1994**

[51] Int. Cl.[6] G06F 9/00

[52] U.S. Cl. 395/568; 395/580

[58] Field of Search 395/163.1, 275, 395/375, 368, 580

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5,253,255	10/1993	Carbine et al. .	
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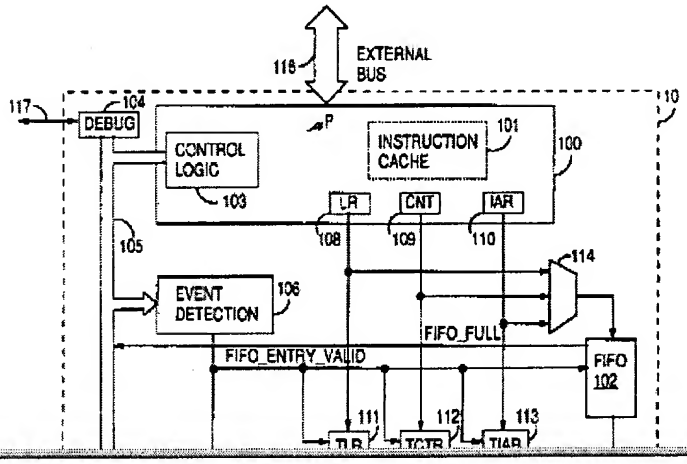
5,442,756	8/1995	Grochowski et al.	395/375
5,488,688	1/1996	Gonzales	395/183.1
5,586,336	12/1996	Nakamura et al.	395/568

Primary Examiner—Jack B. Harvey
Assistant Examiner—David A. Wiley
Attorney, Agent, or Firm—Steven B. Phillips; Jenkins & Gilchrist

[57] **ABSTRACT**

A system and method for tracing program code within a processor having an embedded cache memory. The non-invasive tracing technique minimizes the need for trace information to be broadcast externally. The tracing technique monitors changes in instruction flow from the normal execution stream of the code. The tracing technique monitors the updating of processor branch target register contents in order to monitor branch target flow of the code. A FIFO and serial logic circuitry is utilized to minimize the number of chip pins required to broadcast the information from the chip. The tracing technique utilizes instruction and data breakpoint debug functions to signal an external trace tool that a trace event has occurred.

29 Claims, 6 Drawing Sheets



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Brief Summary Text - BSTX (4):

The increase in use of very large scale integrated ("VLSI") circuit technologies has enabled the integration of entire systems and sub-systems onto a single chip. This integration has led to increased performance on critical processor data and instruction buses through the use of internal data and instruction caches. However, a negative result of this increased integration is a significantly reduced ability to easily access particular buses needed for monitoring processor activity. For instance, an instruction cached design inhibits the ability to monitor and capture the program instruction flow since the instructions are fetched from an embedded cache instead of memory external to the processor. In fact, for efficient cache designs, there is a high probability that the instructions will reside in cache and will not be visible from the external pins of the microprocessor. It is also possible that the entire program may reside in embedded cache, thereby making it virtually impossible to follow instruction execution externally.